CAEN
Tools for Discovery

weeroc

High-end Microelectronics Design

Read-Out Chip Catalog

6345- Catalog

We are proud of the high quality of our products.

ISO 9001

ISO 9001:2015 approved quality system ensures all our internal processes.

From R&D to the registration of the incoming purchase orders, through:
- Resource Planning
- Scheduling
- Production

Our quality system is responsible for the proper functioning of all our internal processes and is subject to regularly audits, carried out by the National Standards Authority.

From the initial product design and its development stages, till the delivery of the production batches, we follow documented procedures that cover every aspect of our business.

The quality of CAEN S.p.A. products is constantly monitored by the application of the UNI EN ISO 9001:2015 standard. CAEN S.p.A. is ISO 9001 certified since 1998.

ISO9001:2015
certified Company

Authorised
research laboratory
of the MIUR

WEEROC

FRONTEND ASICS FOR PARTICLE PHYSICS

CAEN carries the worldwide distribution agreement with Weeroc, the microelectronics company designing front-end readout ASICs for many photodetectors commonly used in physics applications. Weeroc offers a complete range programmable readout chips and associated support for a fast and succesfull integration in the final system.

Wide variety of detectors

Suitable for SiPM, GEMs, Si strip, MA-PMTs and other

RADIOROC
Radioroc is a 64-channel front-end ASIC designed to readout silicon photo-multipliers (SiPM).

Up to 64 channels

High channel density in BGA or QFP form factor, allowing for an ultra-compact and cost-effective design of your experiment

PSIROC
Psiroc is a 64-channel front-end ASIC designed to readout PIN diodes, silicon strips and GEMs, handling detector capacitances ranging from 0 up to few hundreds of pF.

LIROC
Liroc is a 64-channel front-end ASIC designed to readout silicon photomultipliers (SiPM) for LIDAR/fast photon counting.

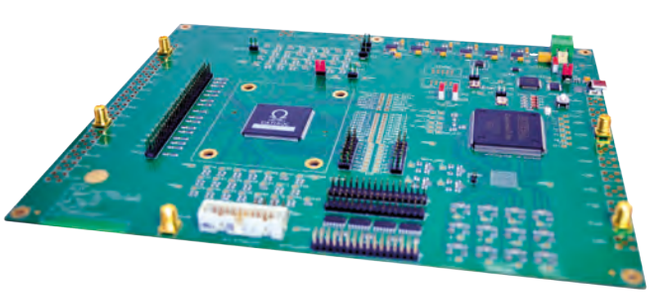
TEMPOROC
Temporoc is a 64-channel front-end ASIC designed to readout silicon photomultipliers (SiPM) in particle time-offlight (TOF) measurement applications.

Testboard available for each ASIC, to evaluate its performances easily and quickly, allowing a versatile use with real detectors

CAEN-Weeroc synergies

CAEN develops readout systems taking advantage of Weeroc ASICs.

Have a look at:
- FERS-5200
- DT5550W
- A1702/DT5702



Testboard

For each of the available ASIC, Weeroc offers a testboard designed to test and characterize the chip. This tool is suited to easily evaluate the performances of the ASIC and, thanks to its features, allows a versatile use with real detectors.

Product lineup

About Weeroc

Weeroc is a fabless microelectronics company designing and providing front-end read-out chips for most of the particle detector or photodetectors. Weeroc offers off-the-shelf programmable read-out chips and associated support for a fast and successful integration of the read-out chip in user system.

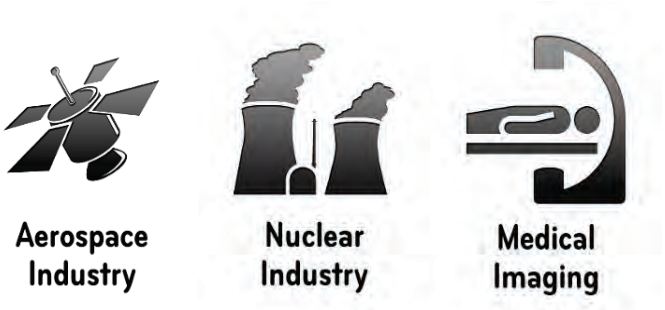
Weeroc designs custom read-out chip on customer request for specific application not covered by programmable component off the shelf.

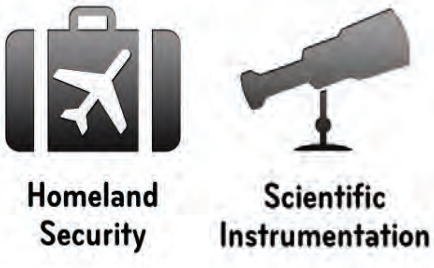
Weeroc's core of design expertise includes low noise and radiation-hardened mixed signal ASICs.

Weeroc is certified ISO9001 since 2015.

Application Domains

Weeroc ASICs are suitable for most industrial or research application involving photodetector or particle detector read-out.





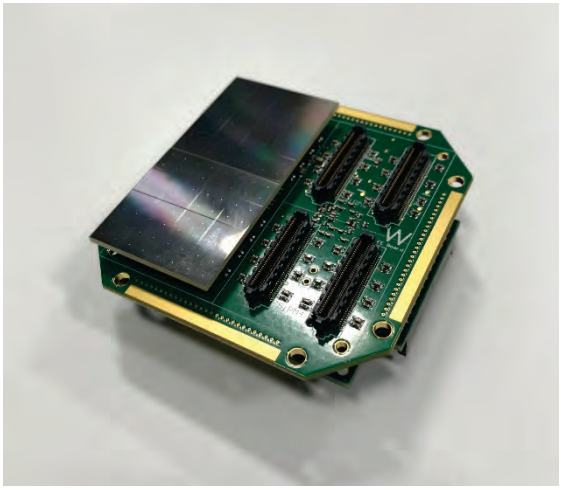
Product lineup

Dedicated Design

Weeroc can design dedicated ASIC for specific application. Non-recurrent design cost are paid by the final customer who have exclusive access to the design he ordered. Typical microelectronics design is 18 months from requirement specification to tested prototypes.

Integration services

Weeroc provide a dedicated front-end board design service to help our customer build their system if no system of the shelf meet their requirements.



Weeroc products maturity is ranged using technical readiness level (TRL) scale. The Weeroc definition of TRL is described below.

Technology Readiness Level	Description
TRL 1	ASIC project
TRL 2	ASIC in foundry
TRL 3	silicon available
TRL 4	First measurements, minor bug detected
TRL 5	First measurement, conclusive in lab
TRL 6	Application prototype available
TRL 7	Full system using ASIC available
TRL 8	Full system using ASIC running
TRL 9	Full system running ASIC, reliability proven

weeroc

	Maroc	Catiroc	Gemroc	Skiroc	Citiroc
Prod. Version	3A	1A	1	2A	1A
TRL	9	8	9	8	9
Package*	PQFP240 TFBGA353	TQFP208	PQFP160	BGA400	PQFP160 TFBGA353
Detector Compatibility	- MA-PMT, PMT - SiPM, SiPM array	- MA-PMT, PMT	- micromegas - GEMs	- Si PIN diodes - Silicon strips	- SiPM - SiPM array
Optimized readout	MA-PMT	PMT	GEMs	Si PIN diodes	SiPM
Channel	64	16	64	64	32
Measurements and operations	- Free running trigger - External trigger - Charge (shaper) - Photon counting - Time (trigger)	- Free running trigger - External trigger - Charge (shaper) - Time (trigger) - Time (TDC)	- Free running trigger - External trigger - Charge (shaper) - Data 3-level trigger	- Free running trigger - External trigger - Charge (shaper) - Time (TDC)	- Free running trigger - External trigger - Charge (shaper) - Time (trigger)
Outputs	- 64 Triggers - Trigger OR - 1 Analog multiplexer (charge) - ADC (8/10/12-bit)	- 16 Triggers - 16 Shapers - Trigger OR - ADC (10-bit) - TDC (10-bit)	- 3 Triggers NOR - 1 Analog multiplexer (charge)	- Triggers NOR - 1 Analog multiplexer (charge) - ADC (12 bit) - TDC (12 bit)	- 32 Triggers - 2 Triggers NOR - 1 Analog multiplexer (charge)
Input Polarity	Negative	Negative	Negative	Positive	Positive
Applications Main features	- Energy meas. - SPE application - Photon counting rate < 30MHz - MA-PMT gain adj.	- Energy meas. - Time stamping - Low dead time - Zero suppress data	- Energy meas. - Time stamping - Data readout: 3-level trigger	- Energy meas. - Time stamping	- Energy meas. - Time of flight - Photon counting - Calibration input - SPE spectrum - Input DAC - SiPM HV adjust.

** QFP packaging will be phased out and replaced with equivalent BGA packaging*

*** BGA516 20x20mm2 – Pin-to-pin compatible*

Glossary: ADC : Analog to Digital Converter – TDC : Time to Digital Converter

Product lineup

Petiroc	Triroc	Radioroc NEW	Psiroc NEW	Liroc NEW	Temporoc NEW
2A	1A	2	1	1	2
6	8	4	4	4	4
TQFP208 TFBGA353	TFBGA353	BGA516**	BGA516**	BGA516**	BGA516**
- SiPM - SiPM array	- SiPM - SiPM array	- SiPM - SiPM array	- PIN Diodes, - Silicon strips, - GEMs	- SiPM - SiPM array	- SiPM - SiPM array
SiPM	SiPM	SiPM	PIN Diodes,	SiPM	SiPM
32	64	64	64	64	64
- Free running trigger - Charge (shaper) - Time (trigger) - Time (TDC)	- Free running trigger - Charge (shaper) - Time (TDC)	- Free running trigger - External trigger - Charge (shaper, ToT) - Time & Charge (trigger) - Photon Counting	- Free running trigger - External trigger - Charge (shaper, ToT) - Time (trigger)	- Free running trigger - Time (trigger) - Photon Counting - Charge (ToT)	- Free running trigger - Charge (shaper) - Time (trigger) - Time (TDC)
- 32 Triggers - Trigger OR - 1Analog multiplexer (charge) - 1 Digital multiplexer (trigger) - ADC (10 bit) - TDC (10 bit)	- 2 Trigger NOR - Analog multiplexer (charge) - 1 Digital multiplexer (trigger) - ADC (10 bit) - TDC (10 bit)	- Selectable per channel: • 1 LVDS trigger • 2 Single ended trigger • 2 Shaper outputs - 3 Triggers NOR - 2 Analog multiplexers	- Selectable per channel: • 1 LVDS trigger • 2 Single ended trigger • 2 Shaper outputs - 3 Triggers NOR - 2 Analog multiplexers	- 64 LVDS trigger outputs	- Trigger OR - 1 Analog multiplexer (charge) - 1 Digital multiplexer (trigger) - ADC (10-bit) - TDC (50 ps)
Negative (optimized) Positive	Negative (optimized) Positive	Positive	Positive, negative	Positive, negative	Positive
- Energy meas. - Time of flight - Time stamping - Photon counting - Input DAC - SiPM HV adjust.	- Energy meas. - Time of flight - Time stamping - Zero suppress data - Input DAC - SiPM HV adjust.	- Energy meas. - Time of flight - Photon counting rate ~100MHz - Dual time thresholds - SPE spectrum - SiPM HV adjust.	- Energy meas.	- Time of flight - Photon counting rate ~300MHz - SPE spectrum - Energy meas. - SiPM HV adjust.	- Energy meas. - Time of flight - Time stamping - Photon counting - Input DAC - SiPM HV adjust.

Maroc 3A

Photomultiplier-tubes read-out chip

MAROC3A is a 64-channel chip designed to readout negative fast input current pulses such as those provided by Multi Anode Photo Multipliers. Each channel provides a 100% trigger rate for signal greater than 1/3 photoelectron (50fC) and a charge measurement up to 30 photoelectrons (~ 5 pC) with a linearity of 2%. The gain of each channel can be tuned between 0 and 4 thanks to an 8-bit variable gain preamplifier allowing to compensate the non- uniformity between detector channels. A slow shaper combined with two Sample and Hold capacitors allows storing the charge up to 5 pC as well as the baseline. In parallel, 64 trigger outputs are obtained thanks to two possible trigger paths: one made of a bipolar or unipolar fast (15 ns) shaper followed by one discriminator for the photon counting and one made with a bipolar fast shaper (with a lower gain) followed by a discriminator to deliver triggers for larger input charges (> 1 pe). The discriminator thresholds are set by two internal 10-bit DACs. A digital charge output is provided by an integrated 8, 10 or 12 bit Wilkinson ADC.

Detector Read-Out	MAPMT, SiPM
Number of Channels	64
Signal Polarity	Negative
Sensitivity	Trigger on 1/3 photo-electron with a 10^6 PM gain or 50 fC
Timing Resolution	60ps RMS on single photo-electron, threshold 1/3 of photo-electron
Dynamic Range	5 pC (10^6 PM gain), Integral Non Linearity: 2% up to 5 pC
Packaging & Dimension	TFBGA353, ~~PQFP240~~ discontinued
Power Consumption	3.5 mW /ch, power supply= 3.3V
Inputs	64 current inputs
Outputs	64 trigger outputs Wired OR of the 64 triggers for each of the 2 discriminators 1 multiplexed analog charge output that can be daisy chained 1 digital charge measurement (8, 10 or 12 bits)
Internal Programmable Features	gain adjustment between 0 and 2 over 8 bits for each input preamp, trigger threshold adjustment (10bits), analog and digital charge measurement, 64 trigger outputs, 64 trigger masks

They are using Maroc 3A

CERN (ATLAS luminometer)
Jefferson lab (CLASS12)
Industrial applications under NDA

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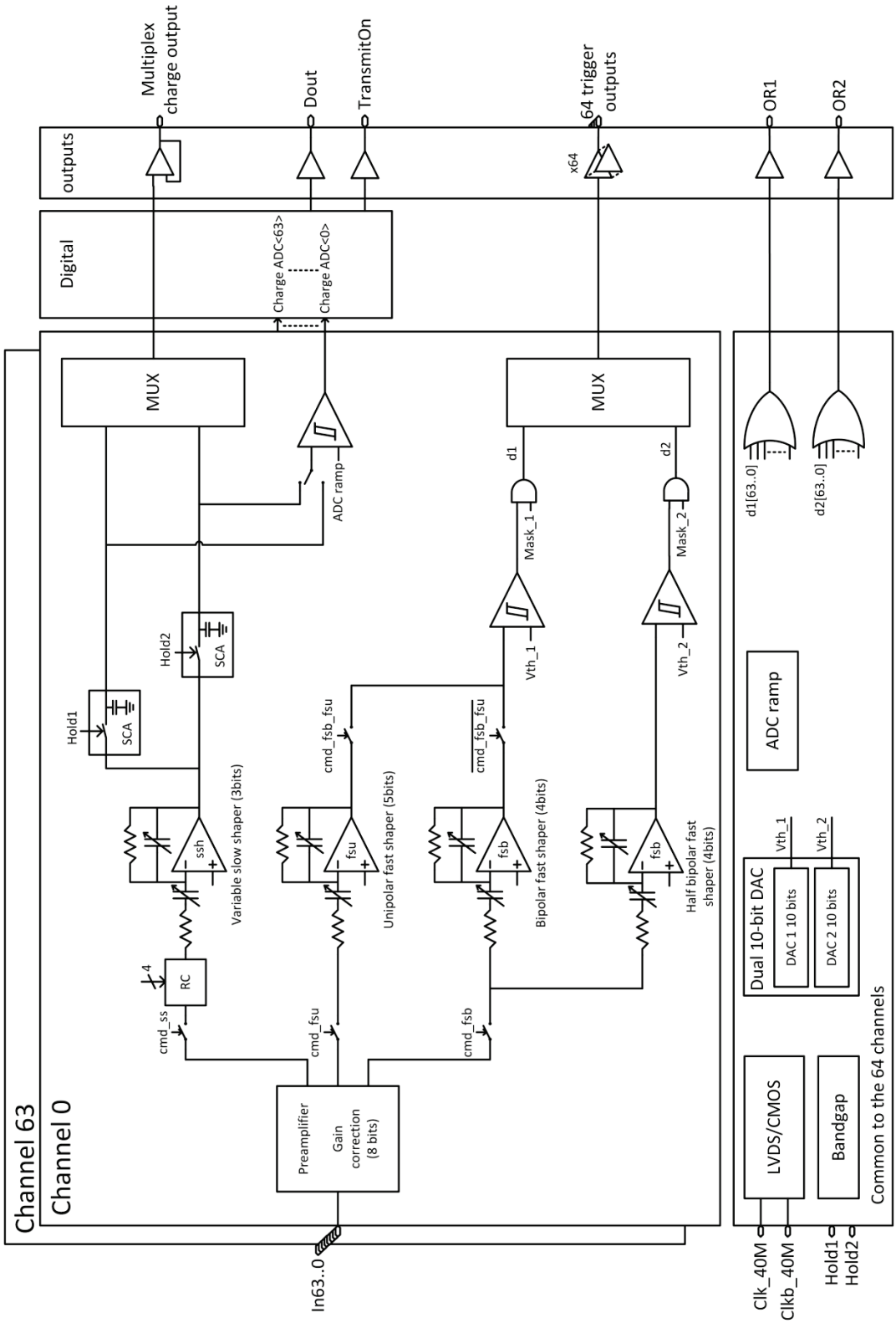
More about Maroc 3A

Maroc 3A

Photomultiplier-tubes read-out chip



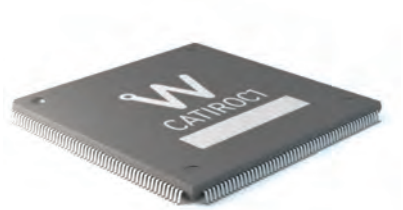
Catiroc 1

Large-Photomultiplier-Arrays Read-Out Chip

CATIROC 1 is a 16-channel front-end ASIC designed to readout photomultiplier tubes (PMTs) in large scale applications such as water Cerenkov experiments. The concept of the ASIC is to combine an auto-trigger chip to 16 PMTs to obtain an autonomous macro-cell for large area of detection.

An adjustment of the gain of each channel compensates for the gain variation of the PMTs and allows using only one HV cable for the 16 PMTs. In the ASIC, the 16 channels are totally independent. In each channel, the auto-trigger starts the charge and time measurements which are then converted and stored. Only the hit channels are read out by one serialized output. The time measurement is done by a 26-bit counter at 40 MHz for the coarse time and a Time to Amplitude Converter (TAC) for the fine time, giving a resolution of 200ps RMS. The charge measurement is done by a dual gain preamplifier followed by a shaper with variable shaping times (25 ns, 50 ns or 100 ns). Charge and fine time values are converted by a 10 bit ADC.

Moreover CATIROC 1 can be used as an analogue front-end ASIC for PMTs. The 16 triggers and 16 shapers output can be used in an application specific optimized front-end board.



Detector Read-Out	PMT, PMT array
Number of Channels	16
Signal Polarity	Negative
Sensitivity	Trigger on one third of photo-electron on each channel
Timing Resolution	200ps RMS on single photo-electron
Dynamic Range	400 photo-electrons (10^6 PMT gain) Integral Non Linearity 1% up to 400 p-e
Packaging & Dimension	TQFP208
Power Consumption	Power supply: 3.3V 21mW/ch.
Inputs	16 voltage inputs
Outputs	16 trigger outputs 16 shaper output 1 or of the 16 trigger output 1 serialized digital data output (50bits/channel)
Internal Programmable Features	16 channel gain adjustment (16x8bits), trigger and gain threshold adjustment (2x10bits), charge measurement tuning, 16 trigger masks, channel by channel trigger output enable.

They are using Catiroc 1

JUNO experiment
WA105 collaboration

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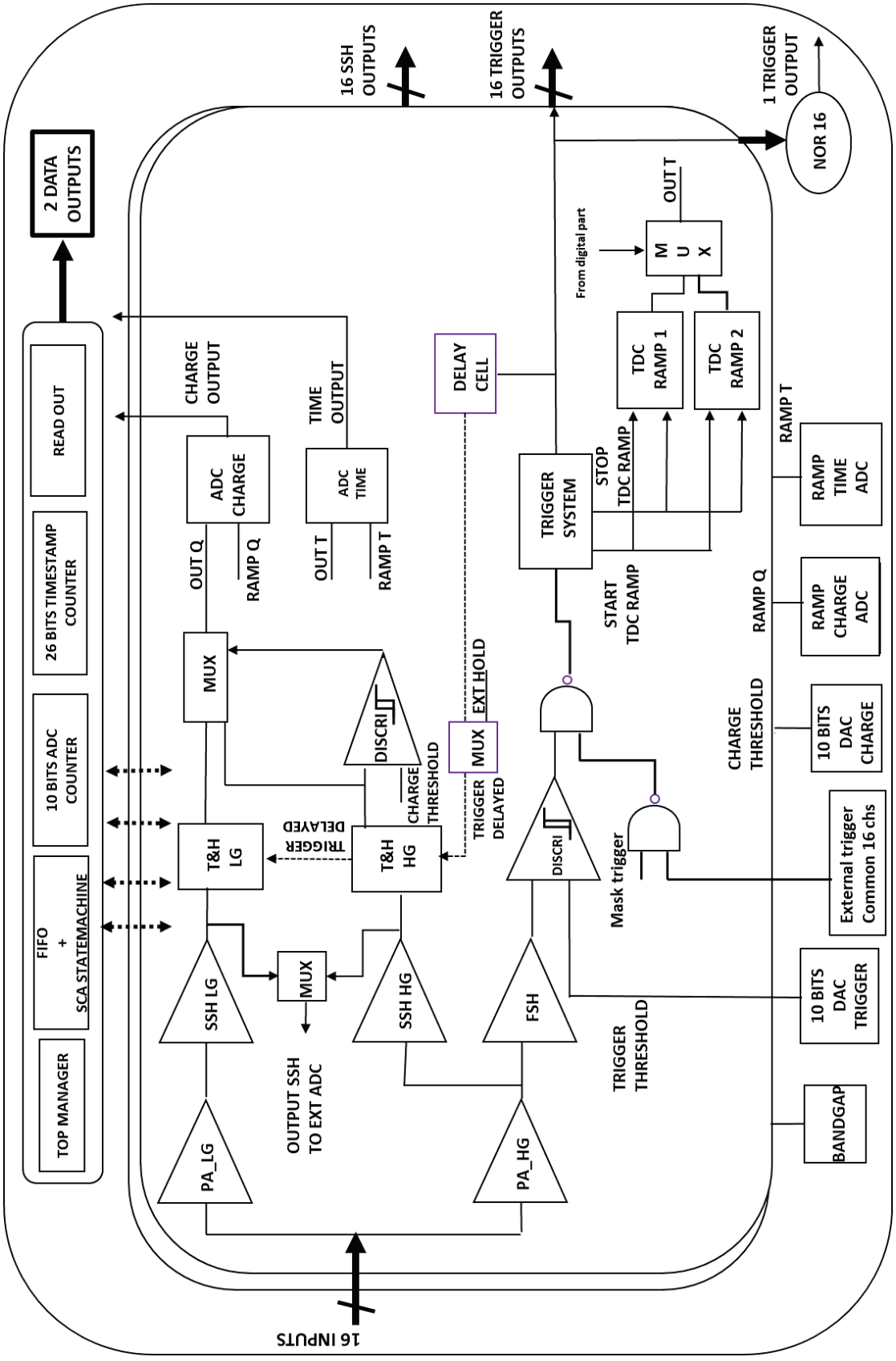
More about Catiroc 1

Catiroc 1

Large-Photomultiplier-Arrays Read-Out Chip



Citiroc 1A

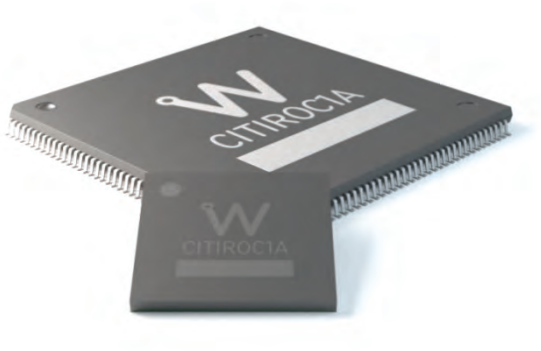
Scientific instrumentation SiPM read-out chip

Citiroc 1A is a 32-channel front-end ASIC designed to readout silicon photo-multipliers (SiPM) for scientific instrumentation application.

Citiroc 1A allows triggering down to 1/3 pe and provides the charge measurement with a good noise rejection. Moreover, Citiroc 1A outputs the 32-channel triggers with a high accuracy (better than 100 ps).

An adjustment of the SiPM high-voltage is possible using a channel-by-channel DAC connected to the ASIC inputs. That allows a fine SiPM gain and dark noise adjustment at the system level to correct for the non-uniformity of SiPMs. Citiroc 1A can be calibrated using a unique calibration signal.

Timing measurement better than 100 ps RMS jitter is possible along with 1% linearity energy measurement up to 2500 p.e. The power consumption 225mW with all stages on.



Detector Read-Out	SiPM, SiPM array
Number of Channels	32
Signal Polarity	Positive
Sensitivity	Trigger on 1/3 of photo-electron
Timing Resolution	Better than 100 ps RMS on single photo-electron
Dynamic Range	0-400 pC i.e. 2500 photo-electrons @ 10^6 SIPM gain
Packaging & Dimension	TQFP 160 – TFBGA353
Power Consumption	225mW – Supply voltage : 3.3V
Inputs	32 voltage inputs with independent SiPM HV adjustments
Outputs	32 trigger outputs 2 multiplexed charge output, 1 multiplexed hit register 2 ASIC trigger output (Trigger OR)
Internal Programmable Features	32 HV adjustment for SiPM (32x8bits), Trigger Threshold Adjustment (10bits), channel by channel gain tuning, 32 Trigger Masks, Trigger Latch, internal temperature sensor

They are using Citiroc 1A

INAF – IASF (CTA experiment)
CERN (Baby mind experiment)

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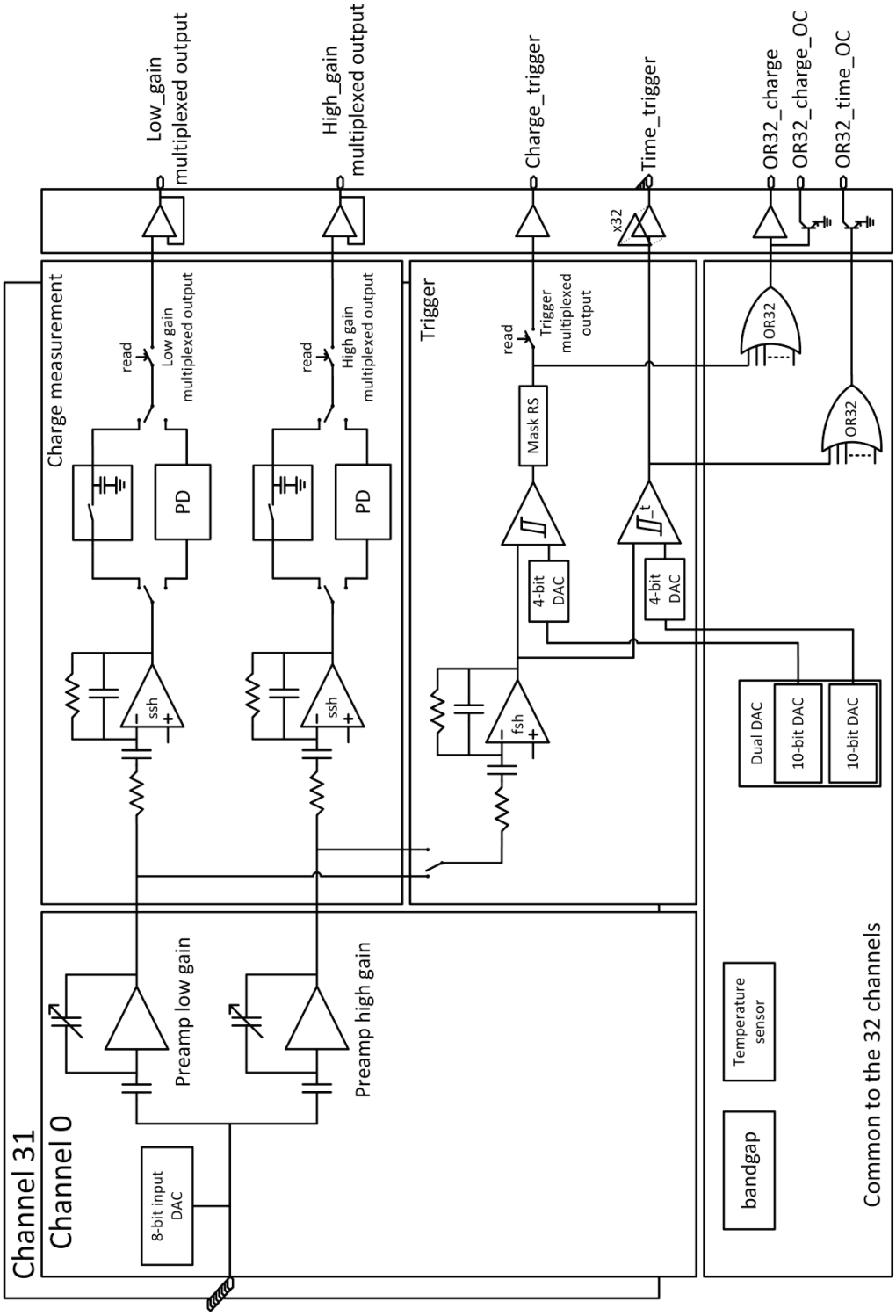
More about Citiroc 1A

Citiroc 1A

Scientific instrumentation SiPM read-out chip



SSH – Slow Shaper ; FSH – Fast Shaper; PD – Peak Detector

Petiroc 2A

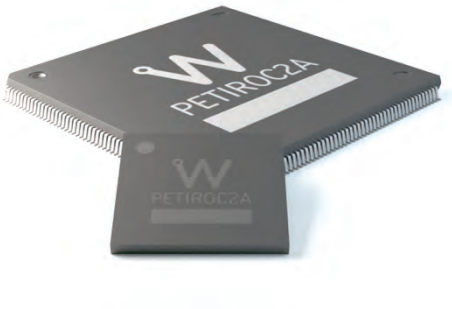
SiPM read-out for time-of-flight PET

Petiroc 2A is a 32-channel front-end ASIC designed to readout silicon photomultipliers (SiPMs) with both polarities for particle time-of-flight measurement applications. Petiroc 2A combines a very fast and low-jitter trigger with accurate charge and time measurements. Energy and time are digitized internally with a 10-bit ADC and 40ps-bin TDC.

The concept of the ASIC is to combine two measurement lines that won't interfere one with each other to measure both first incident photon timing measurement and whole crystal light charge integration.

An adjustment of the SiPM high voltage is possible using a channel-by-channel input DAC. It allows a fine SiPM gain and dark noise adjustment at the system level to correct for the non-uniformity of SiPMs.

The power consumption is 6 mW/channel, excluding buffers used to output the analogue signals. The main application of Petiroc 2A is PET time-of-flight prototyping but it can also be used for any application that requires both accurate time resolution and precise energy measurement.



Detector Read-Out	SiPM, SiPM array
Number of Channels	32
Signal Polarity	Positive or Negative
Sensitivity	Trigger on first photo-electron
Timing Resolution	~ 35 ps FWHM in analogue mode (2pe injected) - ~ 100 ps FWHM with internal TDC
Dynamic Range	3000 photo-electrons (10^6 SIPM gain), Integral Non Linearity: 1% up to 2500 ph-e
Packaging & Dimension	TQFP208 – TFBGA353
Power Consumption	Power supply: 3.3V 192mW Analogue core (excluding analogue outing buffer), 6mW/ch
Inputs	32 voltage inputs with DC adjustment for SiPM HV tuning
Outputs	Digital output (energy on 10 bit, time on 10 bit - 40ps bin) 32 trigger outputs 1 multiplexed charge output, 1 multiplexed hit register 2 ASIC trigger outputs (Trigger OR on 32 channels, 2 levels)
Internal Programmable Features	32 HV adjustment for SiPM (32x8b), trigger threshold adjustment (10b), charge measurement tuning, 32 trigger masks, internal temperature sensor, trigger latch

They are using Petiroc 2A

Industrial applications
Cannot be disclosed

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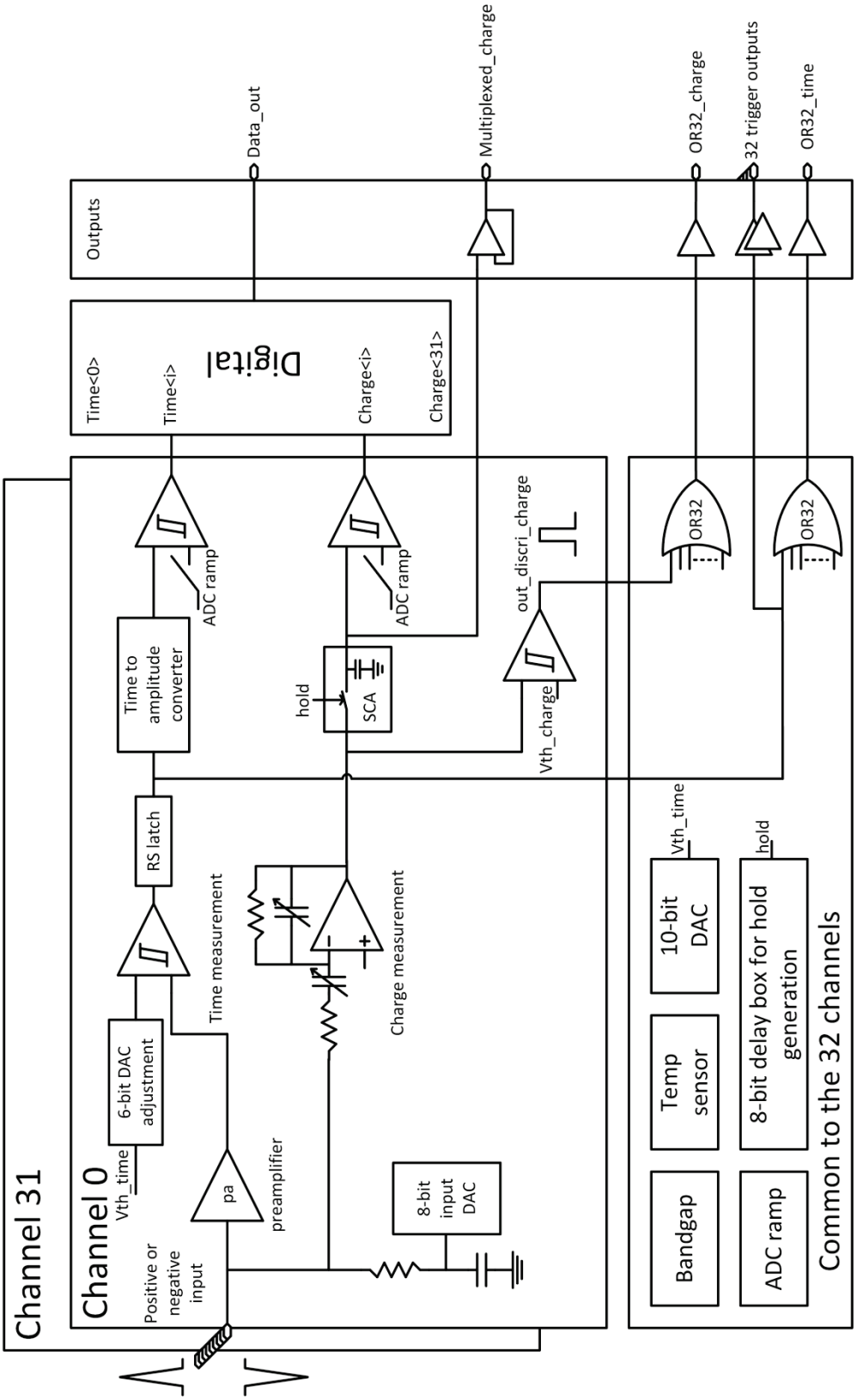
More about Petiroc 2

Petiroc 2A

SiPM read-out for time-of-flight PET



Triroc 1A

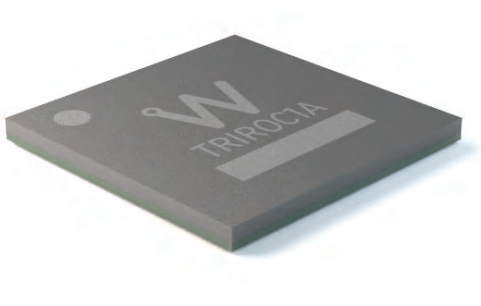
All-in-one SiPM read-out for multimodal PET inserts

Triroc 1A is a 64-channel front-end ASIC designed to readout silicon photomultipliers (SiPMs) with both polarities for particle time-of-flight measurement applications. Triroc 1A combines a very fast and low-jitter trigger with accurate charge and time measurements. Energy and time are digitized internally with a 10-bit ADC and 30ps-bin TDC.

The concept of the ASIC is to combine two measurement lines that won't interfere one with each other to measure both first incident photon timing measurement and whole crystal light charge integration.

An adjustment of the SiPM high voltage is possible using a channel-by-channel input DAC. It allows a fine SiPM gain and dark noise adjustment at the system level to correct for the non-uniformity of SiPMs.

The power consumption is 10 mW/channel, excluding buffers used to output the signals. The main application of Triroc 1A is PET time-of-flight but it can also be used for any application that requires both accurate time resolution and precise energy measurement. Triroc 1A is available in naked dies or BGA packaging (12x12mm, 353 balls).



Detector Read-Out	SiPM, SiPM array
Number of Channels	64
Signal Polarity	Positive or Negative
Sensitivity	Trigger on first photo-electron
Timing Resolution	88 ps RMS
Dynamic Range	3000 photo-electrons (10^6 SIPM gain), Integral Non Linearity: 1% up to 2000 ph-e
Packaging	BGA (12x12mm, 353 balls)
Power Consumption	Power supply: 3.3V 10mW/ch
Inputs	64 voltage inputs with DC adjustment for SiPM HV tuning
Outputs	Digital output (energy on 10 bit, time on 10 bit - 30ps bin) 1 multiplexed time trigger output 2 ASIC trigger OR outputs (64 channels, 2 levels)
Internal Programmable Features	64 HV adjustment for SiPM (64x8bits), trigger threshold adjustment (10bits), charge measurement tuning, ADC Track & Hold/Peak Sensing, 64 trigger masks, internal temperature sensor, trigger latch, Power Pulsing

They are using Triroc 1A

Trimage collaboration (PET/IRM/EEG)
Industrial application
Cannot be disclosed

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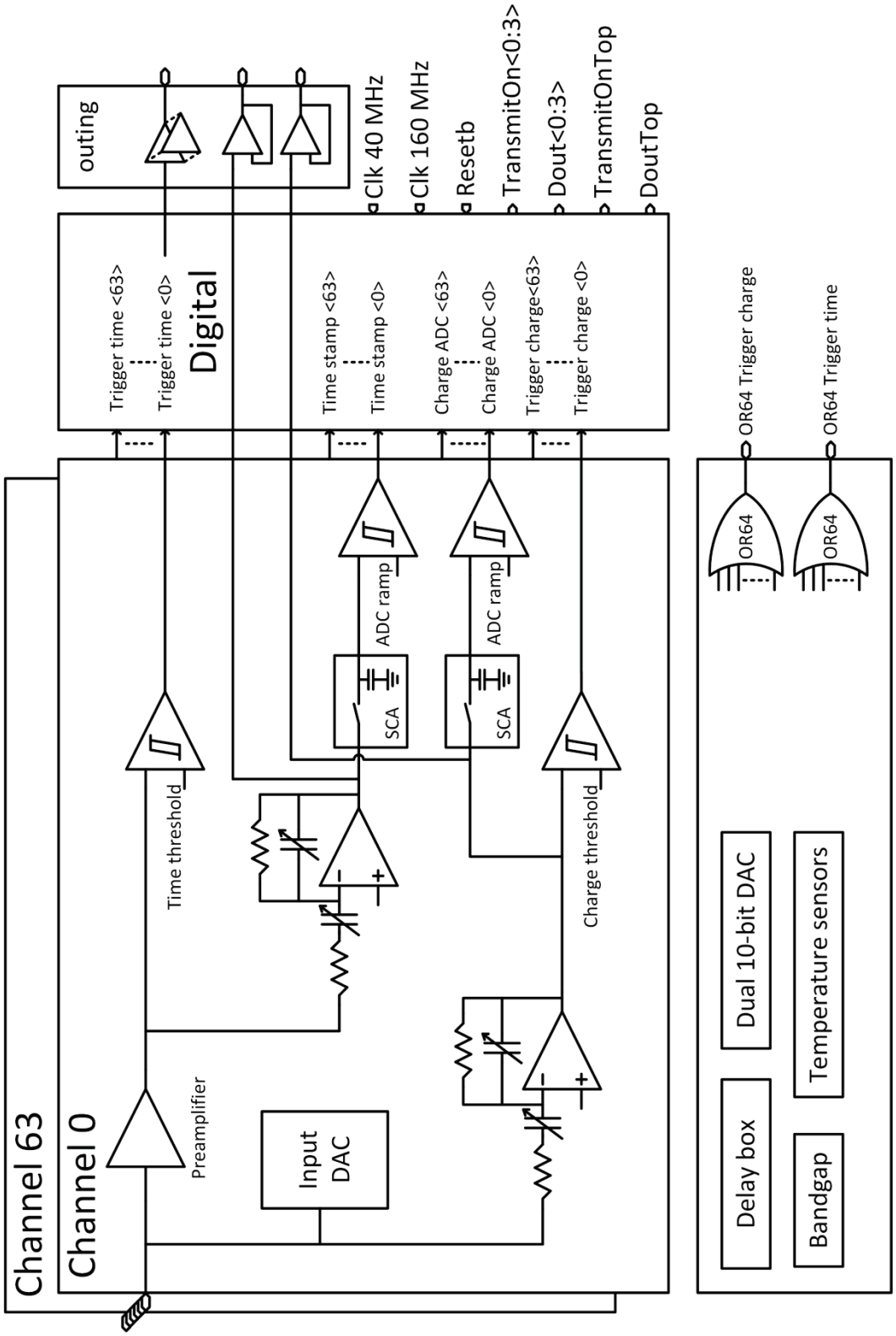
More about Triroc 1A

Triroc 1A

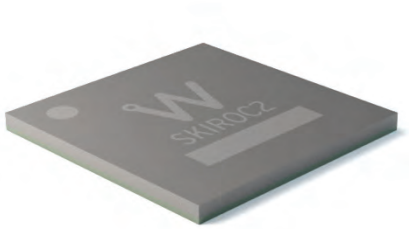
All-in-one SiPM read-out for multimodal PET inserts



Skiroc 2A

PIN Diode and Low Gain Silicium Detector Read-Out Chip

SKIROC 2A is a 64-channel front-end ASIC designed to readout silicon PIN diodes. Each channel is made of a variable-gain and low-noise charge preamplifier followed by two shapers – one with a gain of 1 and the other with a gain of 10 – to provide a charge measurement from 0.2 fC up to 10 pC. A time tagging is performed by a 12-bit TDC ramp. The charges and times are stored in a 15-depth Switched Capacitor Arrays (SCA), the values of which are converted by a multi-channel 12-bit Wilkinson ADC and sent to an integrated 4 Kbytes memory. The analog value of the charge is also available on an output pin. The trigger chain is composed of a high gain fast shaper and a discriminator and allows each channel to auto trigger down to 0.2 fC. Thresholds of the 64 discriminators are set by a common 10-bit DAC and an individual 4-bit DAC per channel. Each discriminator output is sent to an 8-bit delay cell (delay time tunable between 100 ns and 300 ns) to provide the Hold signal for the SCA cells of the slow channel. The power consumption is 6.2 mW/channel and each stage can be individually shut down when not used. 616 slow control parameters are available to set various configurations and ensure the versatility of the chip.



Detector Read-Out	Si PIN Diodes
Number of Channels	64
Signal Polarity	positive
Sensitivity	Trigger on 0.2fC
Timing Resolution	N/A
Dynamic Range	10 pC, Integral Non Linearity <1%
Packaging & Dimension	BGA 400 (17x17mm)
Power Consumption	6.2 mW /ch, power supply: 3.3V power pulsing
Inputs	64 current inputs
Outputs	1 multiplexed analog charge output 12-bit charge and time measurement Trigger OR of the 64 discriminators
Internal Programmable Features	Common gain adjustment for the input, common trigger threshold adjustment (10 bits) and individual threshold (4 b), 12-bit charge and time measurement, 64 trigger masks, multiplexed analog output

They are using Skiroc 2A

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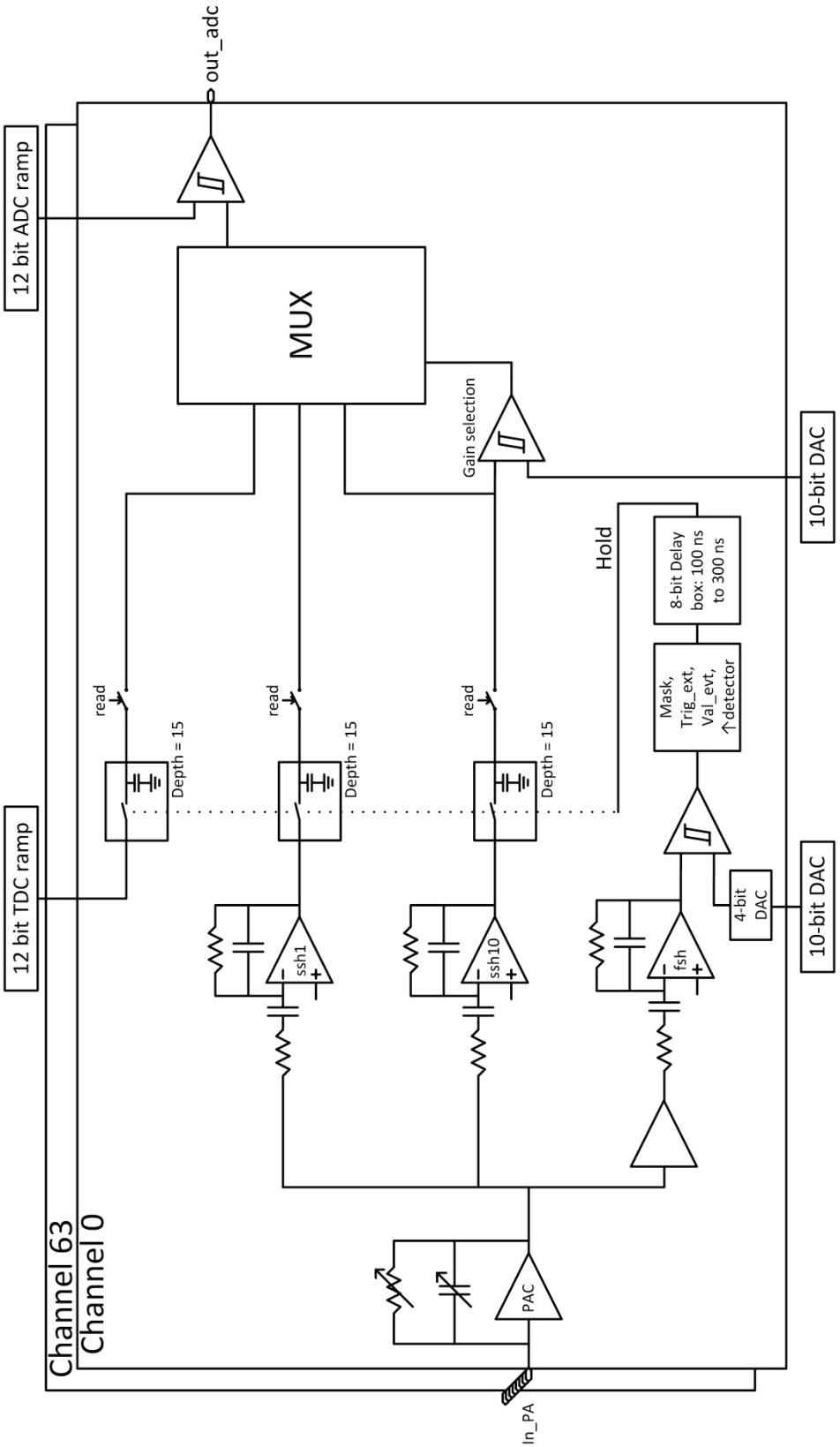
More about Skiroc 2A

Skiroc 2A

PIN Diode and Low Gain Silicium Detector Read-Out Chip



Gemroc 1

Micromegas and GEMs semi-digital read-out chip

GEMROC 1 is a 64-channel front-end ASIC designed to readout negative fast (<1ns) and short (<10ns) current pulses from low gain detectors (GEMs, Micromegas, ...). GEMROC 1 provides a semi-digital readout with three thresholds tunable from 1 fC to 500 fC and integrates a 128-deep digital memory to store the 2 x 64 discriminator outputs as well as the timestamp from a 24b counter. The three thresholds are set internally by three 10-bit DACs. The gain of each channel can be tuned individually from 0 to 2 over 8 bits, allowing the compensation of non-uniformity between the 64 detector channels. Each channel can auto trigger down to 1 fC input charge. A multiplexed charge measurement up to 500fC is integrated.

The power consumption is 1.5 mW/channel and the chip can be fully power-pulsed allowing a significant power reduction by disabling unused blocks.

Detector Read-Out	Micromegas, GEM
Number of Channels	64
Signal Polarity	Negative
Sensitivity	Trigger 1 fC
Timing Resolution	N/A
Dynamic Range	500 fC
Packaging & Dimension	TQFP160
Power Consumption	1.5 mW /ch, power supply: 3.3V power pulsing
Inputs	64 current inputs
Outputs	2 encoded data outputs per channel streamed out in serial 1 multiplexed charge output 3 multiplexed trigger outputs or 3 trigger OR of the 64 channels
Internal Programmable Features	Trigger threshold adjustment (10bits), 3*64 trigger masks, multiplexed latched trigger or direct OR64 trigger outputs

They are using Gemroc 1

Industrial application (NDA)

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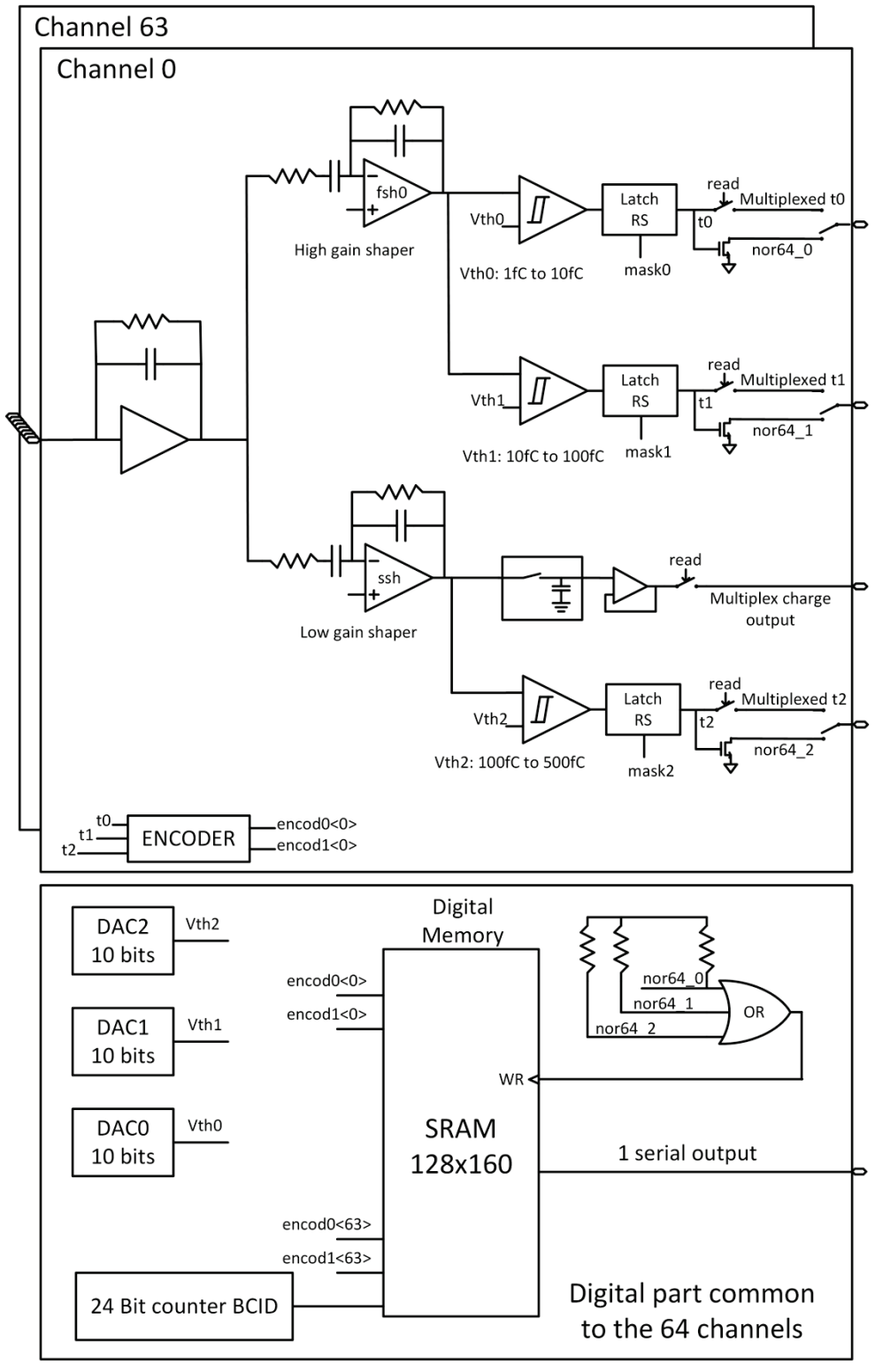
More about Gemroc 1

Gemroc 1

Micromegas and GEMs semi-digital read-out chip



Radioroc 2

Multi-purpose SiPM analogue read-out chip

Radioroc 2 is a 64-channel front-end ASIC designed to readout silicon photo-multipliers (SiPM).

Radioroc 2 allows triggering down to 1/3 p.e. and provides dual-gain energy measurement with excellent Signal-to-noise ratio on the high gain (SNR over 10 for single p.e.) and large dynamic range on the low gain. Moreover, Radioroc 2 can output the 64-channel triggers with jitter expected as low as 35 ps FWHM on a single p.e. (ASIC only). Photo-counting is foreseen over 100 MHz.

An adjustment of the SiPM high-voltage (gain) is possible using a channel-by-channel 8-bit DAC connected to the ASIC inputs. Channel-by-channel calibration on the trigger threshold is also possible thanks to 6-bit DACs. Radioroc can be calibrated using the dark noise of the SiPM.

Timing resolution better than 35 ps FWHM is possible along with 1% linearity energy measurement up to 2000 p.e, the dynamic range being limited by the 1.2 V power supply on the input analogue pad. The power consumption is 3.3 mW per channel.

Detector Read-Out	SiPM, SiPM array
Number of Channels	64
Signal Polarity	Positive
Sensitivity	Trigger on 1/3 photo-electron
Timing Resolution	Better than 55 ps FWHM on single photo-electron (measured)
Dynamic Range	up to 2000 photo-electron @ 106 SiPM gain - Peaking time from 20ns to 2us for PSD
Packaging & Dimension	FC-BGA 516 20x20mm (Low-inductance flip chip)
Power Consumption	310 mW supply voltage 1.2V
Inputs	64 analogue inputs with independent SiPM HV adjustments
Outputs	2 outputs per channel, either: - 64 LVDS triggers - 2 x 64 TTL triggers - 64 TTL triggers and 64 analog outputs 2 multiplexed analogue outputs 3 NOR64 trigger outputs channels
Internal Programmable Features	64 HV adjustment for SiPM (64 x 8 bits) 3 trigger threshold tuning (10bits) Channel-by-channel gain and shaping time adjustment (τ = 20 ns to 300 ns) Individual trigger masking and cell powering.

NEW

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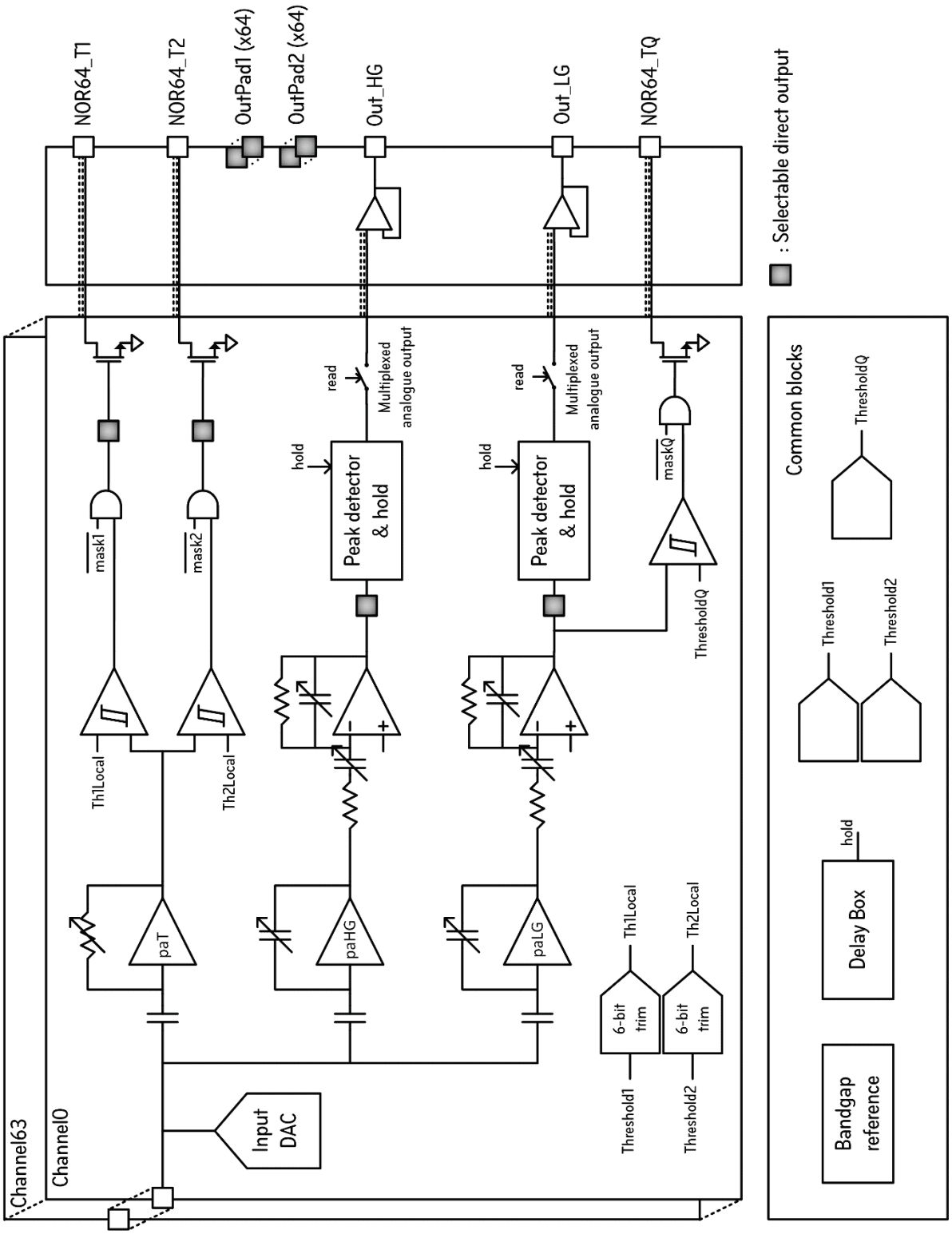
More about Radioroc 2

weeroc

Radioroc 2

Multi-purpose SiPM analogue read-out chip



weeroc

Psiroc 1

PIN Diodes, Silicon Strips and GEMs read-out chip

Psiroc is a 64-channel front-end ASIC designed to readout PIN diodes, silicon strips and GEMs, handling detector capacitances ranging from 0 up to few hundreds of pF.

Psiroc allows triggering down to 0.5 fC on sub-20pF detector capacitances and provides dual-gain energy measurement with excellent Signal-to-Noise Ratio on the high gain (SNR over 10 for 0.5 fC) and large dynamic range on the low gain. For input signals over few pC a channel-wise ToT output is also available. Psiroc can be programmed to output the shapers HG/LG, individual triggers or ToT signals (two output pins per channels). The preamplifier gain is adjustable from 125 mV/pC up to 4 V/pC.

Charge measurement is done with peak detectors but those can be used in a track & hold fashion thanks to an internal delay cell. Analog data are outputted on two multiplexed analog output and can be read-out with an external ADC. Shapers shaping time can be adjusted from 20 ns to 3 µs with a step of 20 ns up to 300 ns and a step of 200 ns up to 3 µs. Data acquisition can be done ASIC wide or channel-wise.

Channel-by-channel calibration on the trigger thresholds for time trigger and ToT can be done with individual 6-bit DACs.

Detector Read-Out	PIN Diodes, Silicon strips, GEMs
Number of Channels	64
Signal Polarity	Positive, negative
Sensitivity	Trigger on 0.5 fC on both polarity
Timing Resolution	< 150 ps RMS @ Qin = 4 fC ; Cd/Cf = 20p/1p (pa gain = 1 V/pC)
Dynamic Range	Up to 5 pC with low gain charge measurement and up to 100 pC with ToT
Packaging & Dimension	FC-BGA 516 20x20mm (Low-inductance flip chip)
Power Consumption	350 mW supply voltage 1.2V
Inputs	64 analogue inputs
Outputs	2 outputs per channel, either: - 64 LVDS triggers - 2 x 64 TTL triggers - 64 TTL triggers and 64 analog outputs 2 multiplexed analogue outputs 3 NOR64 trigger outputs channels
Internal Programmable Features	3 trigger threshold tuning (10bits) channel-by-channel gain and shaping time adjustment (τ = 20 ns to 3 µs) individual trigger masking and cell powering.

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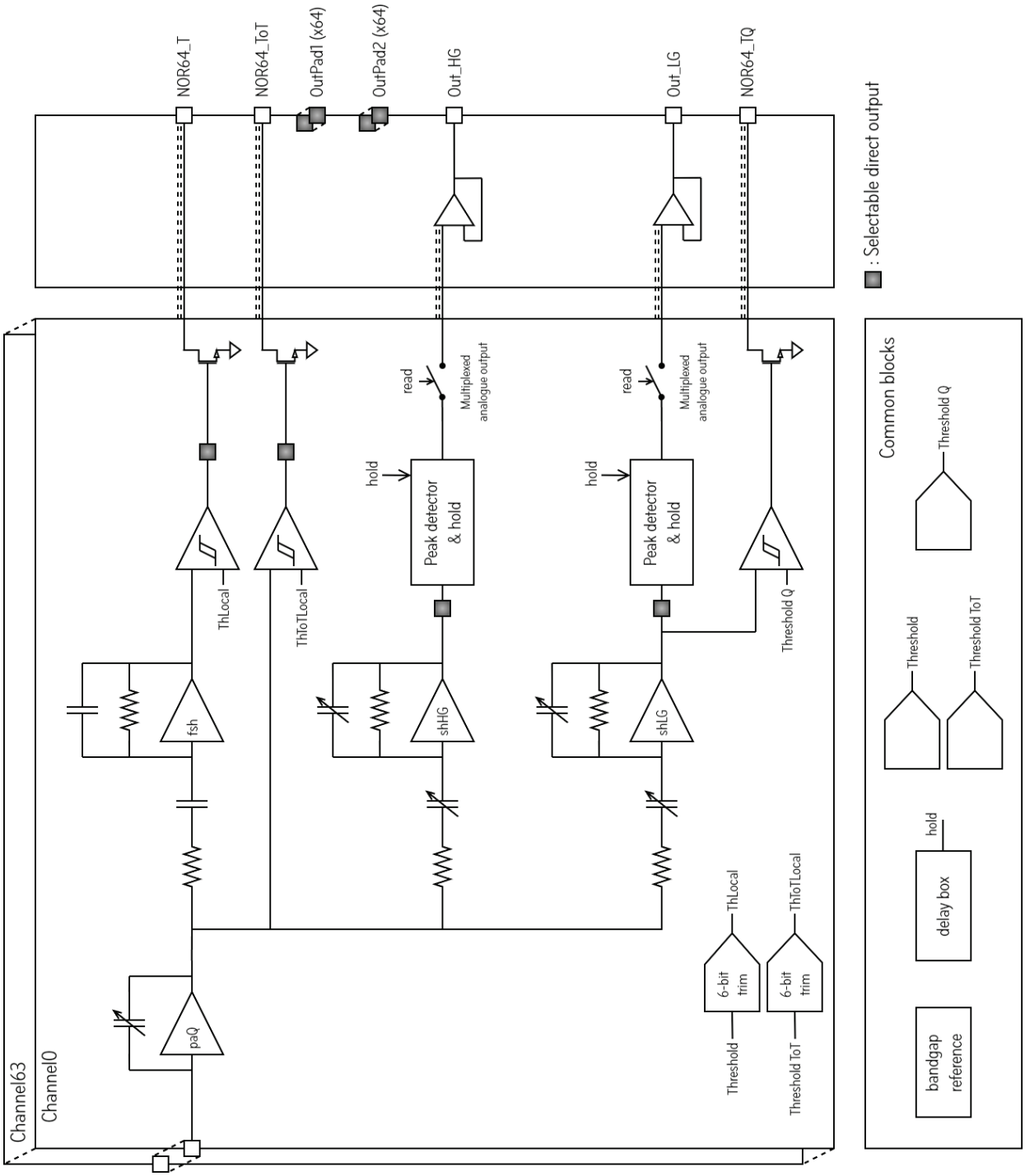
More about Psiroc 1

Psiroc 1

PIN Diodes, Silicon Strips and GEMs read-out chip



weeroc

Liroc 1

SiPM-based LIDAR read-out chip

Liroc is a 64-channel front-end ASIC designed to read-out silicon photo-multipliers (SiPM) for LIDAR application.

Liroc allows triggering down to 1/3 p.e. and provides low-voltage differential trigger output for each channel with an excellent timing resolution (better than 20ps FWHM) and excellent double-peak separation (100% efficiency on 5ns separated single photo-electrons). Liroc allows fast single photon counting over 100MHz per channel.

An adjustment of the SiPM high-voltage (gain) is possible using a channel-by-channel 6-bit DAC connected to the ASIC inputs. Channel-by-channel calibration on the trigger threshold is also possible thanks to 7-bit DACs. Liroc can be calibrated using the dark noise of the SiPM.

Liroc features a GHz measurement line composed of an RF preamplifier with pole zero cancellation followed by a fast discriminator and low swing LVDS fast driver.

Detector Read-Out	SiPM, SiPM array
Number of Channels	64
Signal Polarity	Both Positive and Negative
Sensitivity	Trigger on 1/10 photo-electron
Timing Resolution	Double peak separation: better than 5 ns on single photo-electron Time resolution: better than 20 ps FWHM on single photo-electron
Dynamic Range	up to 15 photo-electron with ToT @ 10^6 SiPM gain
Packaging & Dimension	FC-BGA 516 20x20mm (Low-inductance flip chip)
Power Consumption	640 mW supply voltage 1.2V
Inputs	64 analogue inputs with independant SiPM HV adjustments
Outputs	Digital output (dual ADC and dual TDC per channel) – selectable transmission mode. 1 multiplexed time trigger output 2 ASIC trigger OR outputs (64 channels, 2 levels)
Internal Programmable Features	64 HV adjustment for SiPM (64x8bits) time trigger threshold adjustment (10bits) charge measurement tuning ADC Peak Sensing 64 trigger masks channel by channel output enable, trigger latch programmable data output.

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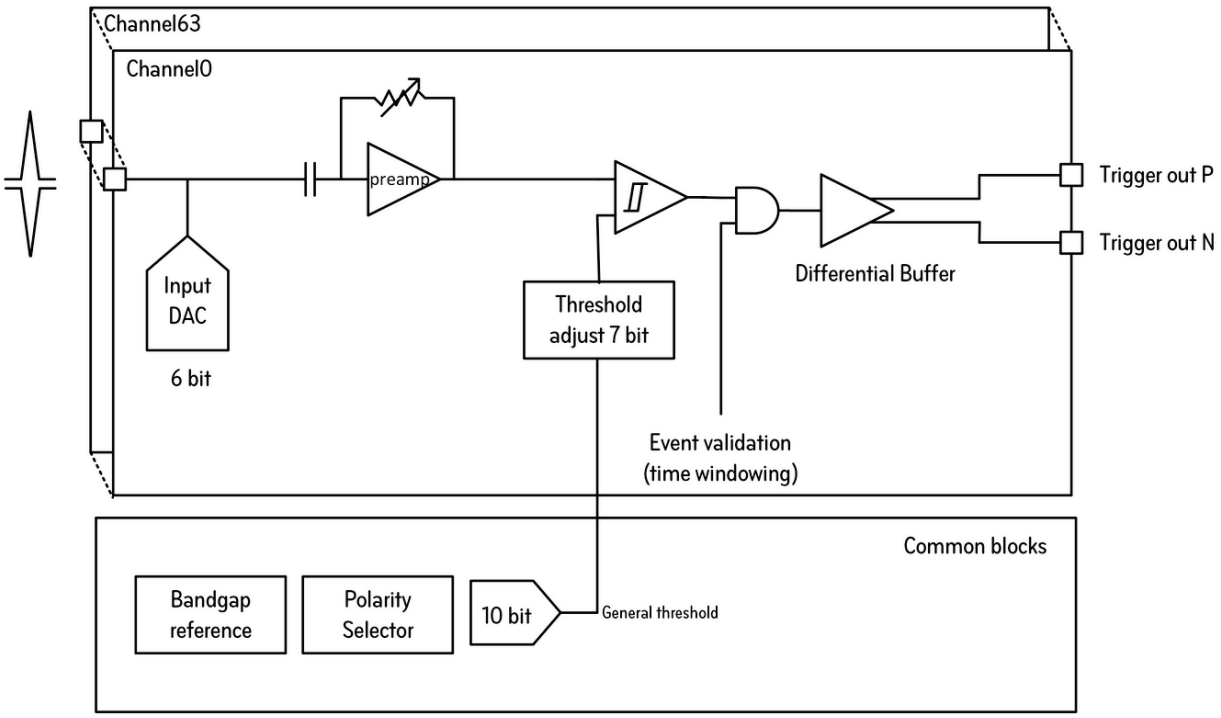
More about Liroc 1


Channel63
Channel0
preamp
Input DAC
6 bit
Threshold adjust 7 bit
Event validation (time windowing)
Differential Buffer
Trigger out P
Trigger out N
Common blocks
Bandgap reference
Polarity Selector
10 bit
General threshold

Temporoc 2

Multi-Purpose Mixed-Signal SiPM read-out chip

Temporoc 2 is a 64-channel front-end ASIC designed to readout silicon photomultipliers (SiPMs) for particle time-of-flight measurement applications. Temporoc 2 combines a very fast and low-jitter trigger with accurate charge and time measurements. Energy and time are digitized internally with a 10-bit ADC and 50ps-bin TDC. In total, Temporoc 2 is capable of providing two distinct time tagging and two energy measurement of each event.

The concept of this ASIC is combining two measurement lines that won't interfere one with each other to measure both first incident photon timing measurement and whole crystal light charge integration. Additionally, Temporoc 2 features clustering triggers readout which could be useful for particle detection with monolithic scintillator.

An adjustment of the SiPM high voltage is possible using a channel-by-channel input DAC. It allows a fine SiPM gain and dark noise adjustment at the system level to correct for the non-uniformity of SiPMs.

The power consumption is 10 mW/channel, excluding buffers used to output the signals. Temporoc 2 is suitable for any application that requires both accurate time resolution and precise energy measurement such as time-of-flight gamma detection.

Detector Read-Out	SiPM, SiPM array
Number of Channels	64
Signal Polarity	Positive
Sensitivity	Trigger on 1/3 photo-electron
Timing Resolution	Better than 20 ps RMS on single photo-electron
Dynamic Range	up to 3000 photo-electron @ 10^6 SiPM gain
Packaging & Dimension	FC-BGA 516 20x20mm (Low-inductance flip chip)
Power Consumption	640 mW supply voltage 1.2V
Inputs	64 analogue inputs with independant SiPM HV adjustments
Outputs	Digital output (dual ADC and dual TDC per channel) – selectable transmission mode. 1 multiplexed time trigger output 2 ASIC trigger OR outputs (64 channels, 2 levels)
Internal Programmable Features	64 HV adjustment for SiPM (64x8bits) time trigger threshold adjustment (10bits) charge measurement tuning ADC Peak Sensing 64 trigger masks channel by channel output enable, trigger latch programmable data output.

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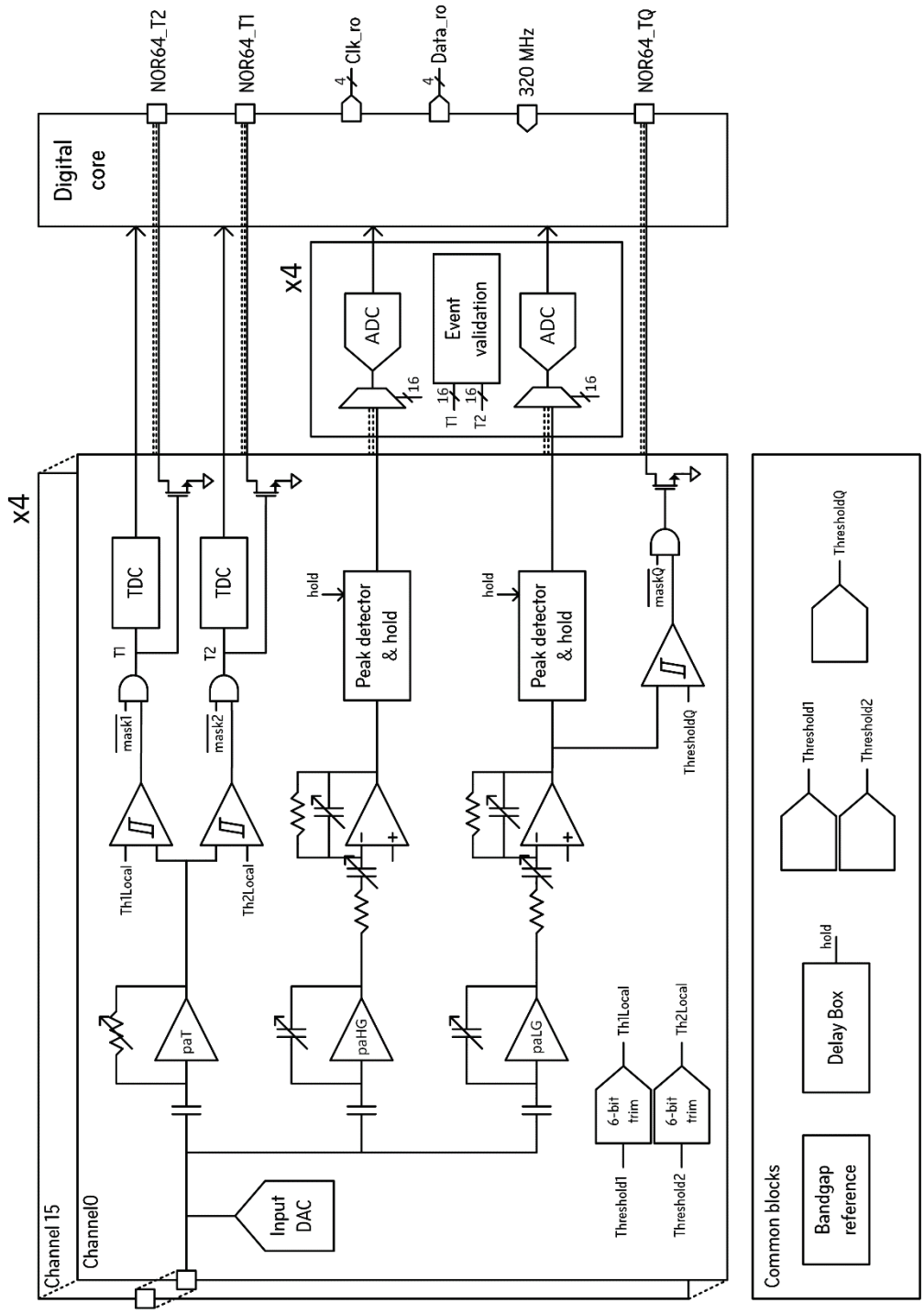
More about Temporoc 2

Temporoc 2

Multi-Purpose Mixed-Signal SiPM read-out chip



FERS-5200

Modular, scalable and synchronized set of electronics surrounding your experiment and reading out thousands of detectors!

FERS-5200 is a Front-End Readout System designed to read out large arrays of detectors, such as SiPMs, multi-anode PMTs, Silicon Strip detectors, Wire Chambers, GEM, Gas Tubes and others.

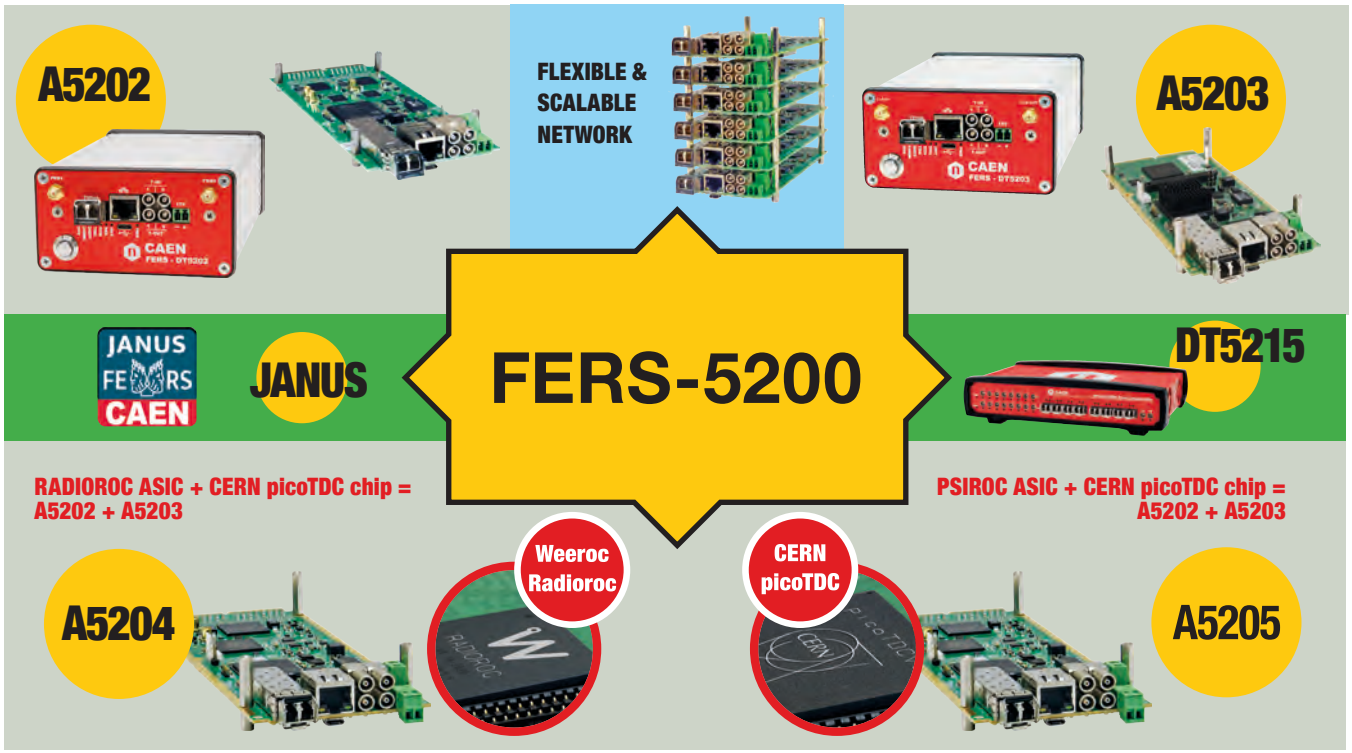
FERS is a distributed and easy-scalable platform, where each unit is a small card that houses 64 or 128 channels with Front End electronics, synchronization, local memory and readout interface.

Multiple FERS units can be connected in a tree network thanks to the DT5215 Concentrator Board, that exploits the optical TDlink (a CAEN proprietary protocol) as the unique physical connection that guarantees high throughput data readout, slow control and accurate timing synchronization.

FERS has been created keeping flexibility in mind: a single user-interface and readout infrastructure has been designed to support and perform a wide range of front-end tasks suitable for a large variety of detector types.

MAIN FEATURES

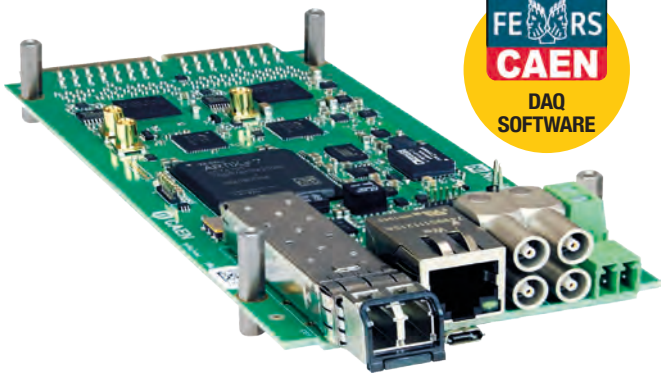
- Platform for the readout of large arrays of detectors (SiPM, MA-PMTs, Gas Tubes, Si detectors, ...)
- Versatility: a family of Front-End cards (FERS units) tailored for different detectors
- Scalability: from a single standalone FERS unit for prototyping to many thousands of channels, with simple tree network structure
- Modularity: multiple FERS units can be distributed on a large detector volume and managed by a single Concentrator board
- Flexibility: possibility to fit different front-end in the same architecture
- Compactness: front-end cards with high channel density ASICs and effective connection to the detector backplane
- Easy-synch: optical link (TDlink) daisy-chain for data readout, slow control and boards synchronization
- Concentrator Board with 8 TDlink
- Boxed FERS unit for desktop use or naked for customizable mechanical frames



A5202/DT5202

64 CH READOUT AND BIAS FOR SILICON PHOTOMULTIPLIERS

A5202 DT5202



JANUS FERS CAEN DAQ SOFTWARE

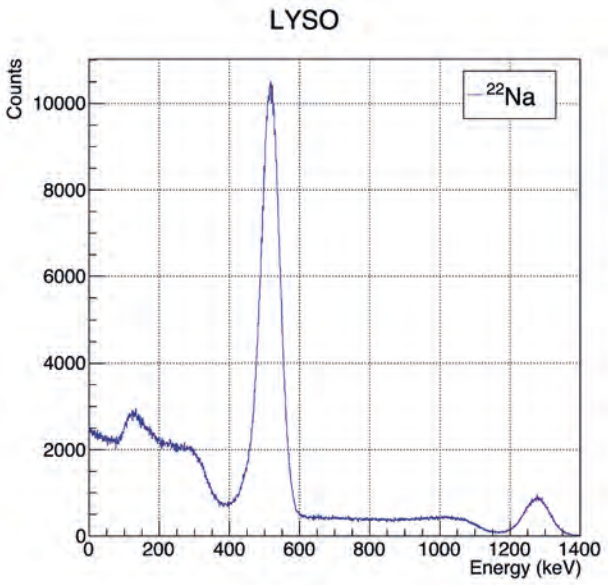
SiPM | 10/100 MbE | TDLINK | USB 2.0 | WEB INTERFACE

Ideal to read out large arrays of SiPM. Full compatibility with 64-pixel matrices

The A5202 is a small board (~ 7 cm x 17 cm) housing two Citiroc-1A chips (64 readout channels). Each readout channel is composed of a Preamplifier, a Slow Shaper with pulse height detector, and a Fast Shaper followed by a discriminator. Pulse height values from each Citiroc-1A are converted sequentially by a 13-bit ADC to perform energy measurements. The 64 channel self-triggers (discriminator outputs) can be used for counting, time stamping, to determine the Time over Threshold (ToT) information, and also to generate the board bunch trigger that starts the ADC conversion. The A5202/DT5202 board also integrates the A7585D power supply module necessary for biasing the SiPMs, and the interfaces for readout, synchronization, and control.

The Janus 5202 software, allowing to completely manage the A5202/DT5202 module and the data acquisition, is also provided for free by CAEN.

The offer is completed by a useful set of cables and adapters to connect different kind of SiPMs and possibly remote them, to enable easy fitting into any real setup.



Landau distribution of cosmic rays measured with the A5202 using coincidence trigger logic.

ACCESSORIES

Input adapters:

- A5250 - 2.54 mm pin header adapter (included with DT5202 model)
- A5251 - Hamamatsu MPPC adapter
- A5253 - 3-pin adapter for single-pixel SiPMs
- A5254 - SensL ArrayJ adapter

Cables:

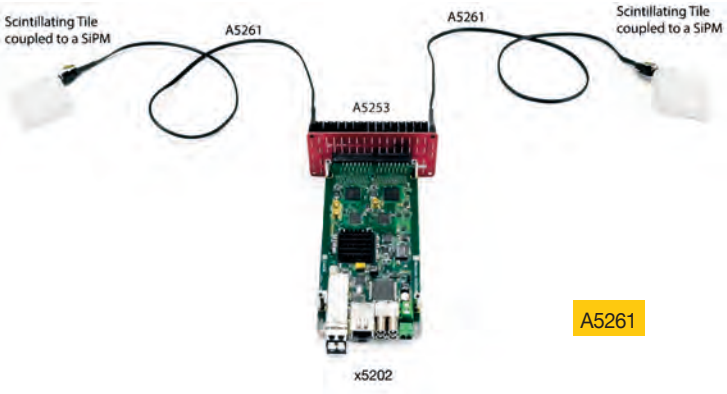
- A5260 - Remotization cable for FERS-5200 boards - 50 cm
- A5260B - Remotization cable for FERS-5200 boards - 100 cm
- A5261 - SiPM remotization cable (70 cm) for A5253

FAN

- A5270 - FERS cooling fan

REMOTIZATION KITS AND ADAPTERS available for maximum flexibility!

A5260



A5261

A5203 DT5203

JANUS FERS CAEN DAQ SOFTWARE

A5203/DT5203

64/128 CH TDC WITH 3.125 ps LSB RESOLUTION

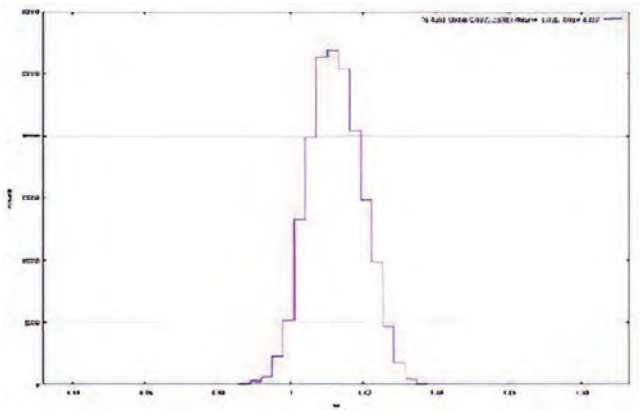
The best achievable timing resolution in a compact form factor and optional dual-threshold discriminators

The A5203 is a small board (~ 7 cm x 17 cm) housing a CERN picoTDC ASIC, featuring 64/128 digital inputs for time measurements. Each readout channel can accept LVDS signals and measure their rising/falling edge timestamps. In this way, the unit is able to reconstruct Time of Arrival of signals as an absolute timestamp or as a deltaT with respect to a common Tref pulse, as well as the Time over Threshold that allows for amplitude estimation or walk correction.

Typical RMS resolution is 7 ps(*).

The Janus 5203 software, allowing to completely manage the A5203/DT5203 module and the data acquisition, is also provided for free by CAEN.

The offer is completed by a useful set of adapters to easily connect signals with flat cables to the high-density input edge-connector of the A5203. Moreover, the A5256 adapter allows to use 16+1 analog/digital single-ended signals on LEMO connectors and discriminate them thanks to the embedded fast voltage comparators with programmable threshold.



(*) Spectrum of ΔT between ch1 and ch0 in Common Start Mode, measured with a pulse generator, 1 V single-ended pulse, 0.8 ns rising edge using the A5255 adapter. The RMS resolution is nearly 7 ps.

ACCESSORIES

Input adapters:

- A5255 - Quad 17x4 Header Adapter (included with DT5203 model)
- A5256 - 16+1 ch. Pos/Neg Discriminator for A5203

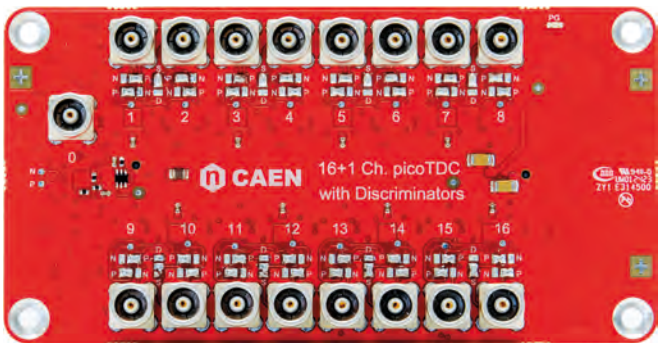
Cables:

- A5260 - Remotization cable for FERS-5200 boards - 50 cm
- A5260B - Remotization cable for FERS-5200 boards - 100 cm

FAN

- A5270 - FERS cooling fan

A5256



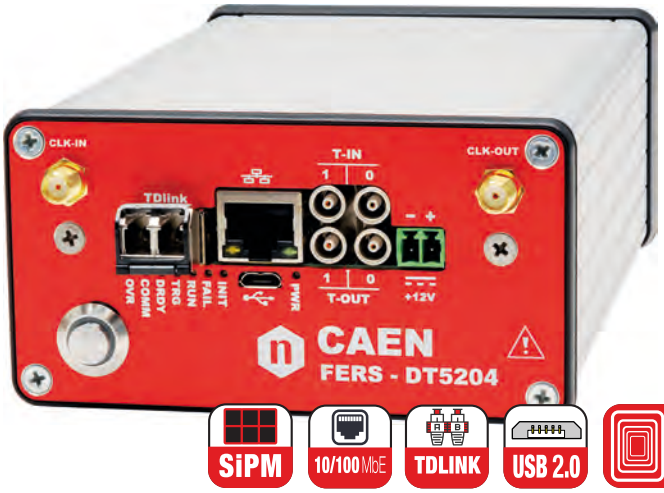
16+1 channel single threshold, or 8+1 channel dual threshold, leading edge discriminator for analog signals available!

A5204/DT5204

64 CHANNEL RADIOROC UNIT FOR FERS-5200

JANUS FERS CAEN DAQ SOFTWARE

A5204 DT5204



SiPM 10/100 MbE TDLINK USB 2.0 WEB INTERFACE

Radioroc and picoTDC chips synergy for unparalleled resolution in energy and time

The A5204 is a small board (~7x20 cm^2) housing one Weeroc Radioroc ASIC and one CERN picoTDC chip, featuring 64 analog inputs.

Besides a slow shaper with a pulse height detector for the data acquisition, the Radioroc ASIC includes configurable fast pre-amplifiers followed by fast shapers and discriminators that can output 64 individual channel triggers with jitter as low as 55 ps FWHM on a single p.e. The individual channel triggers are connected to the FPGA, for photo-counting up to 200 MHz as well as for the implementation of coincidences, majority and topological acquisition triggers. The individual triggers are also connected to the picoTDCchip, thet allows for very precise timing measurements thanks to the 3.125 ps LSB. Time over Threshold (ToT) can also be used to estimate the pulse height, making it possible to acquire time stamp and PHA with very low dead time and extremely high rate, without the need of the multiplexed A/D conversion.

The A5204/DT5204 integrates the A7585D power supply module for the SiPM biasing, and the interfaces for readout, synchronization and control.

Janus 5204 Open Source software on Windows® and Linux® is provided for free by CAEN for an easy management of the board configuration and data acquisition.

As for the other FERS-5200 units, the A5204/DT5204 present a wide range of accessories: adapters and cables specifically designed to provide versatility of choice and the ability to remotely operate the detectors.

ACCESSORIES

Input adapters:

- A5250 - 2.54 mm pin header adapter for A5202/DT5202 & A5204/DT5204
- A5251 - Hamamatsu MPPC header adapter for A5202/DT5202 & A5204/DT5204
- A5253 - 3-pin header adapter for A5202/DT5202 & A5204/DT5204
- A5254 - OnSemi (ex SensL) ARRAY J/C header adapter for A5202/DT5202 & A5204/DT5204

Cables:

- A5260 - Remotization cable for FERS-5200 boards
- A5261 - SiPM remotization cable (0.7 m) for A5253

FAN

- A5270 - FERS cooling fan

A5205 DT5205

A5205/DT5205

64 CHANNEL PSIROC UNIT FOR FERS-5200

COMING SOON

Designed to readout PIN diode, silicon strip and GEM detectors

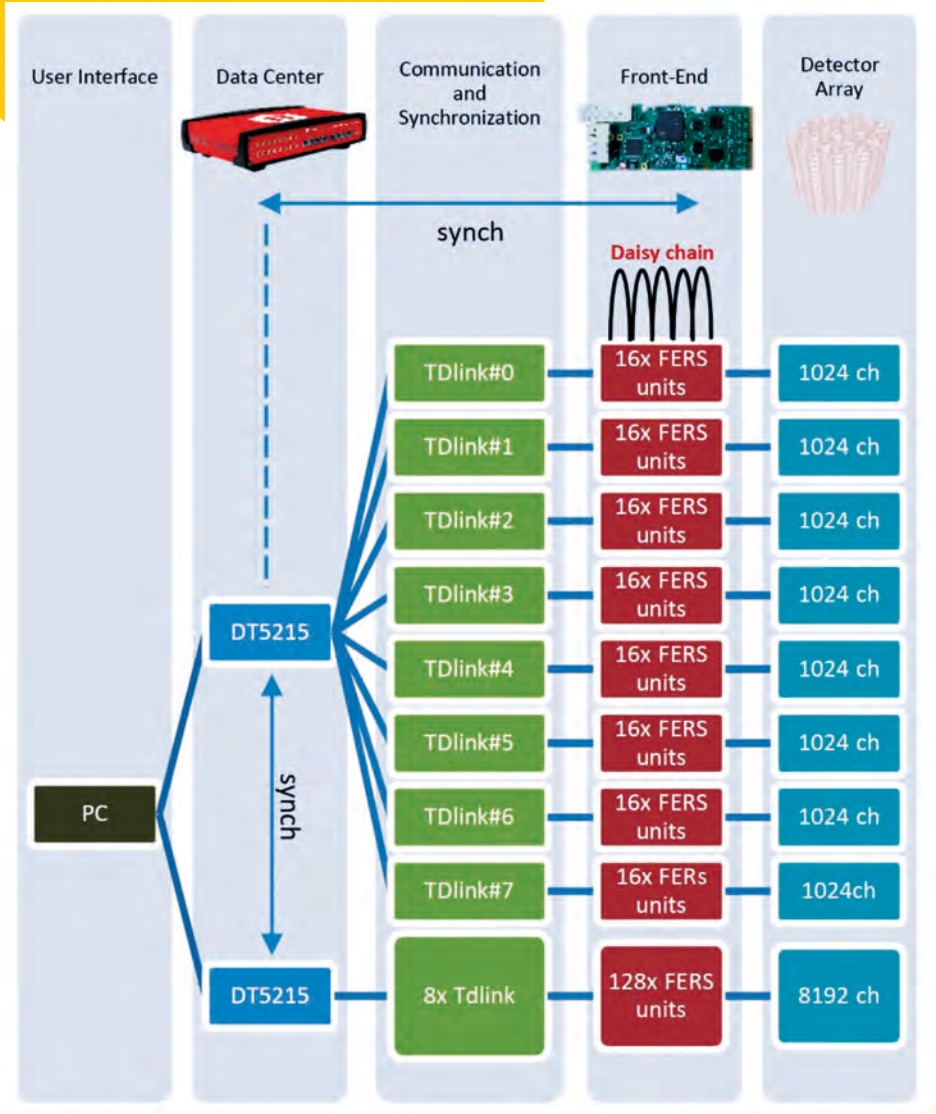
The new A5205/DT5205 FERS unit is designed to readout PIN diodes, silicon strips and GEM detectors, thanks to the coupling Weeroc Psiroc ASIC and CERN picoTDC chip. The small ~7x20 cm2 board features 64 analog inputs, accepting both positive and negative signal polarities. Charge measurements are performed with peak detectors on a pre-amplified and shaped charge signal. Psiroc chip allows for adjustable preamplification gain from 125 mV/pC up to 4 V/pC and triggering down to 0.5 fC on sub-20pF detector. For input signals over few pC a channel-wise Time over Threshold (ToT) output is also available.

Data acquisition can be common to all channels or channel-wise. The individual triggers are also connected to the picoTDC chip, that allows for very precise timing measurements thanks to the 3.125 ps LSB. ToT can also be used to estimate the pulse height, making it possible to acquire time stamp and PHA with very low dead time and extremely high rate, without the need of the multiplexed A/D conversion.

The A5205/DT5205 integrates the interfaces for readout, synchronization and control. Janus 5205 Open Source software on Windows® and Linux® is provided for free by CAEN for an easy management of the board configuration and data acquisition. As for the other FERS-5200 units, the A5205/DT5205 presents a wide range of accessories: adapters and cables specifically designed to provide versatility of choice and the ability to remotely operate the detectors.

DT5215

CONCENTRATOR BOARD FOR FERS-5200



The DT5215 Concentrator Board is responsible for synchronization and data collection from multiple FERS units. It features 8 optical TDLink connectors, each with the possibility of controlling up to 16 FERS units in daisy-chain, for a total of 128 cards per concentrator. Multiple concentrator boards can be synchronized in order to further extend the total number of channels.

The Concentrator is the core of DAQ, picking up the fragments acquired by each unit and sending them sorted and merged to the host PC. A Linux-based Single Board Computer is embedded in the Concentrator board. It manages the data readout from the network of FERS units and the event data building according to the time stamp and/or trigger ID of the event fragments acquired by each unit. Sorted and merged data packets are then stored in the local memory and finally sent to the host computers through a fast 10 GbE or USB 3.0 link. Custom algorithms for data processing and reduction can be easily uploaded by the user into the embedded CPU.

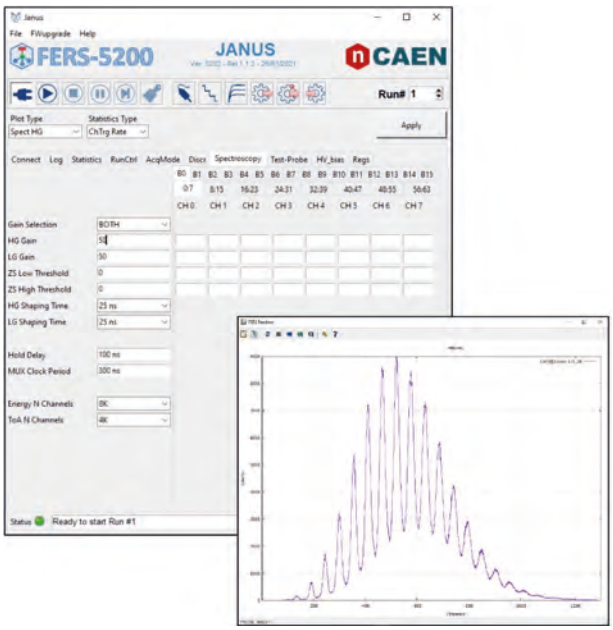
JANUS

FERS-5200 DAQ SOFTWARE

A single DAQ software to control the FERS-5200 board family. Available in Console and GUI Mode, it allows the user to customize the DAQ, and offers an easy way to approach multi-boards and high-channel density FERS-5200 systems.

Janus is an open source software for the control and readout of FERS-5200 boards. Available in two versions (Ver. 5202, Ver. 5203), it can be used as a platform for the development of custom DAQ, tailored to the specific application. Indeed, the user can change the data treatment, the acquired statistics and the output file format.

Janus can manage up to 16 FERS units connected via Ethernet or USB directly as well as the readout of the DT5215 Concentrator Board, so that a single user interface is available for the whole system.



Janus is composed of two parts, one written in C, which is the real heart of the application, one written in Python which manages the user interface. The plots are executed through Gnuplot. All the configuration parameters are written in a textual configuration file.

It is possible to launch and use Janus in 2 different modes:

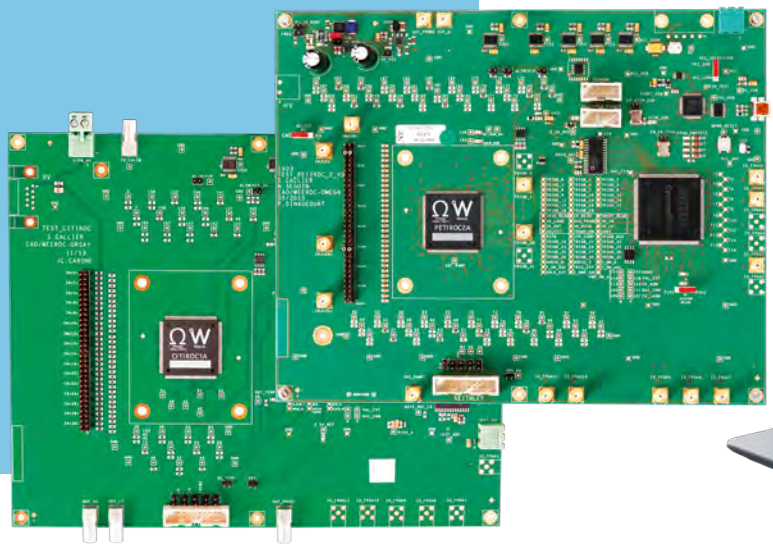
- **Console Mode.** In this case, the Python part of the software is not used. The user can edit the configuration file with any text editor and save the proper values for the desired parameters. Then, the user can launch a purely textual console window. The application writes a series of messages (which are also saved in a log file) and, during the run, prints statistics on the screen. The only graphical part is the plot, which is managed by Gnuplot.
- **GUI Mode**: In this case, the user only have to run the Python program which calls the C program and connects to it via a socket to send commands and receive messages which are then displayed in the Python GUI.

Features

- Model-dependent GUI for a quick and easy start
- Open-Source for user customization
- Management of the acquisition parameters of all connected boards
- Multi parametric Jobs and Runs with time or counts preset
- Data saving of lists in .bin, .txt format
- Statistics and Plots visualization

Weeroc Testboards

Control Systems for Weeroc ASICs



A simple way to learn the use of Weeroc ASICs

Features

- Specific design for each Weeroc ASIC
- Hosting a small ASIC for easy DAQ management
- Easy characterization and debug of the ASIC
- Access to all ASIC's digital and analog I/Os
- ASIC internal signals monitor
- Data acquisition with real detectors
- Connections for an external High Voltage power supply
- Mini-USB for data transfer and board power supply
- Control and acquisition software for Windows OS (LabVIEW interface for TRIROC 1A board)

Overview

Weeroc Testboards are compact form factor platforms designed to control and read out Weeroc ASICs. This tool is suited to easily evaluate the characteristics of the ASIC and, thanks to its features, allows a versatile use with real detectors. The testboard provides easy access to all ASIC's digital and analog I/Os and implements a DAQ system consisting of an Altera Cyclone III FPGA and 12-bit ADCs.

The board hosts connections for detectors and the relative High Voltage distribution lines. Moreover, it provides the possibility to inject signals in the ASIC analog inputs using a generator.

A dedicated software for each different ASIC is available. It provides a simple GUI to set all the programmable parameters of the ASIC and allows the user to perform calibration and DAQ in an intuitive way. Some firmware options can also be set in order to manage DAQ within an experiment..

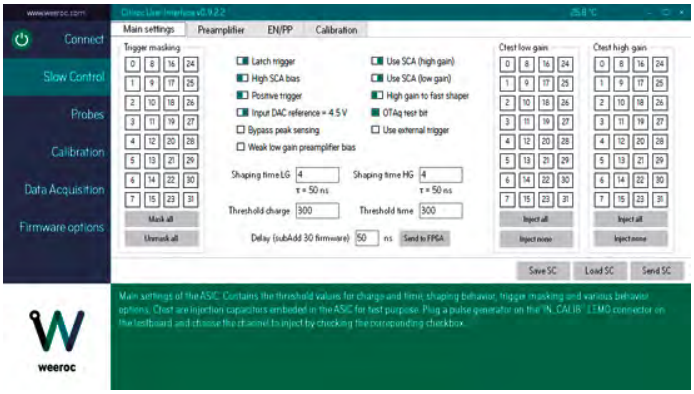
Software

Testboard Software

FREE

For each different testboard, a dedicated User Interface software for Windows OS is available for free download. It provides a simple GUI to set all the programmable parameters of the ASIC and allows the user to perform calibration and DAQ. Some firmware options can also be set.

The TRIROC testboard is equipped with a LabVIEW User Interface.



ORDERING OPTION

WEEROC

Read-Out Chips

Code	Description
WWMAROC3ABAA	MAROC 3A - Photomultiplier tubes read out chip - BGA (Ball Grid Array)
WWCATIROC1QA	CATIROC 1 - Large photomultiplier arrays read out chip - QFP (Quad Flat Pack)
WWCITIROC1AB	CITIROC 1A - Scientific instrumentation SiPM read out chip - BGA (Ball Grid Array)
WWCITIROC1AQ	CITIROC 1A - Scientific instrumentation SiPM read out chip - QFP (Quad Flat Pack)
WWPETIROC2AB	PETIROC 2A - SiPM read out for time of flight PET - BGA (Ball Grid Array)
WWPETIROC2AQ	PETIROC 2A - SiPM read out for time of flight PET- QFP (Quad Flat Pack)
WWTRIROC1ABA	TRIROC 1A - All in one SiPM read out for multimodal PET inserts - BGA (Ball Grid Array)
WWSKIROC2ABA	SKIROC 2A - PIN diode and low gain silicium detector read out - BGA (Ball Grid Array)
WWGEMROC1QAA	GEMROC 1 - Micromegas and GEMs semi digital read out chip - QFP (Quad Flat Pack)
WWLIROC1BAAA	LIROC 1 SiPM Analogue Read-out Chip for Lidar and Photon Counting Application
WWRADIO2BAAA	RADIOROC 2 Dual Read-Out(Photon Counting & Charge Integration) Multi-Purpose SiPM Analogue Chip
WWPSIROC1BAA	PSIROC 1 - PIN Diodes, Silicon Strips amnd GEMs Read-Out Chip
WWTBCATIROC1	Testboard for CATIROC 1 QFP chip
WWTBCITIROC1	Testboard for CITIROC 1A BGA chip
WWTBGEMROC1A	Testboard for GEMROC 1 QFP chip
WWTBMAROC3AA	Testboard for MAROC 3A BGA chip
WWTBPETIROC2	Testboard for PETIROC 2A BGA chip
WWTBTRIROC1A	Testboard for TRIROC 1A BGA chip
WWTBSKIROC2A	Testboard for SKIROC 2A BGA chip
WWTBLIROC1BA	Testboard for LIROC 1 BGA chip
WWTBRADIO2BA	Testboard for RADIOROC 2 BGA chip
WWTBPSIROC1B	Testboard for PSIROC 1 BGA chip

FERS

A5202/DT5202+Adapters & Cables p. 43

Code	Description
WA5202XAAAAA	A5202 - 64 Channel Citiroc unit for FERS-5200
WDT5202XAAAA	DT5202 - Desktop 64 Channel Citiroc unit for FERS-5200
WA5250FHAXAA	A5250 - 2.54 mm pin header adapter for FERS-5200
WA5251FMAXAA	A5251 - MPPC header adapter for A5202/DT5202
WA5253F3AXAA	A5253 - 3-pin header adapter for FERS-5200
WKA5253X64AA	A5253 Kit - A5253 adapter and 64 SiPM remotization CABLES
WA5254FSAXAA	A5254 - SensL ArrayJ Adapter for A5202/DT5202
WA5260XAAAAA	A5260 - Remotization cable for FERS-5200 boards - 50 cm
WA5260BXAAAA	A5260B - Remotization cable for FERS-5200 boards - 100 cm
WA5261XAAAAA	A5261 - SiPM remotization cable (0.7 m) for A5253
WA5270FANXAA	A5270 - FERS cooling fan

A5203/DT5203+Adapters & Cables p. 44

Code	Description
WA5203XAAAAA	A5203 - 64 Channel pico-TDC unit for FERS-5200
WA5203BXAAAA	A5203B - 128 Channel pico-TDC unit for FERS-5200
WDT5203XAAAA	DT5203 - Desktop 64 Channel pico-TDC unit for FERS-5200
WA5255XAAAAA	A5255 - Quad 17x4 Header Adapter
WA5256XAAAAA	A5256 - 16+1 ch pos/neg Discriminator for A5203
WA5260XAAAAA	A5260 - Remotization cable for FERS-5200 boards - 50 cm
WA5260BXAAAA	A5260B - Remotization cable for FERS-5200 boards - 100 cm
WA5270FANXAA	A5270 - FERS cooling fan

A5204/DT5204 p. 45

Code	Description
WDT5204BXAAA	DT5204B – Desktop 64 channel Radioroc unit for FERS
WDT5204XAAAA	DT5204 – Desktop 64 channel Radioroc unit for FERS-5200 with picoTDC

A5205/DT5205 p. 46

Code	Description
WDT5205BXAAA	DT5205B – Desktop 64 channel Radioroc unit for FERS
WDT5205XAAAA	DT5205 – Desktop 64 channel Radioroc unit for FERS-5200 with picoTDC

DT5215 p. 47

Code	Description	Form Factor
WDT5215XAAAA	DT5215 - Collector Board for FERS-5200	Desktop

weeroc

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weeroc

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