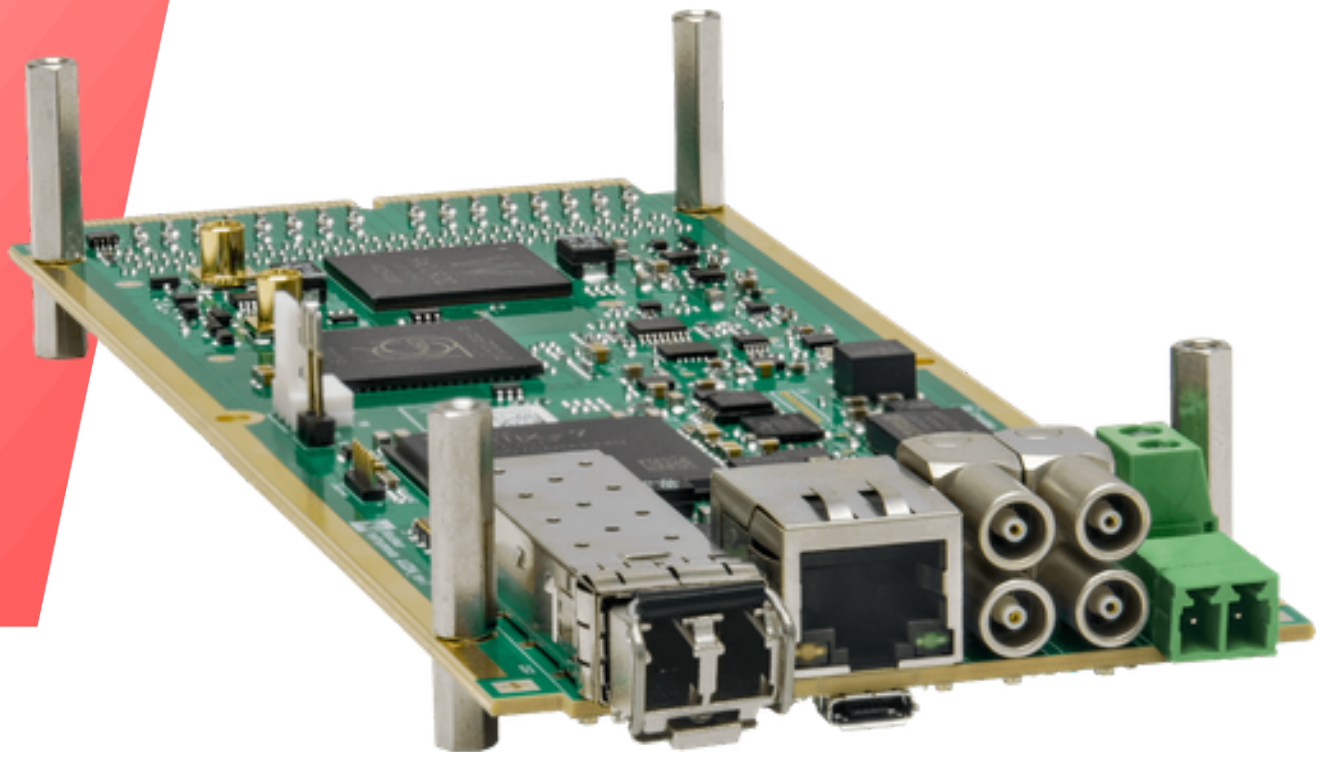
CAEN
Tools for Discovery

Coming Soon

A5205

64 Channel Psiroc Unit for FERS-5200



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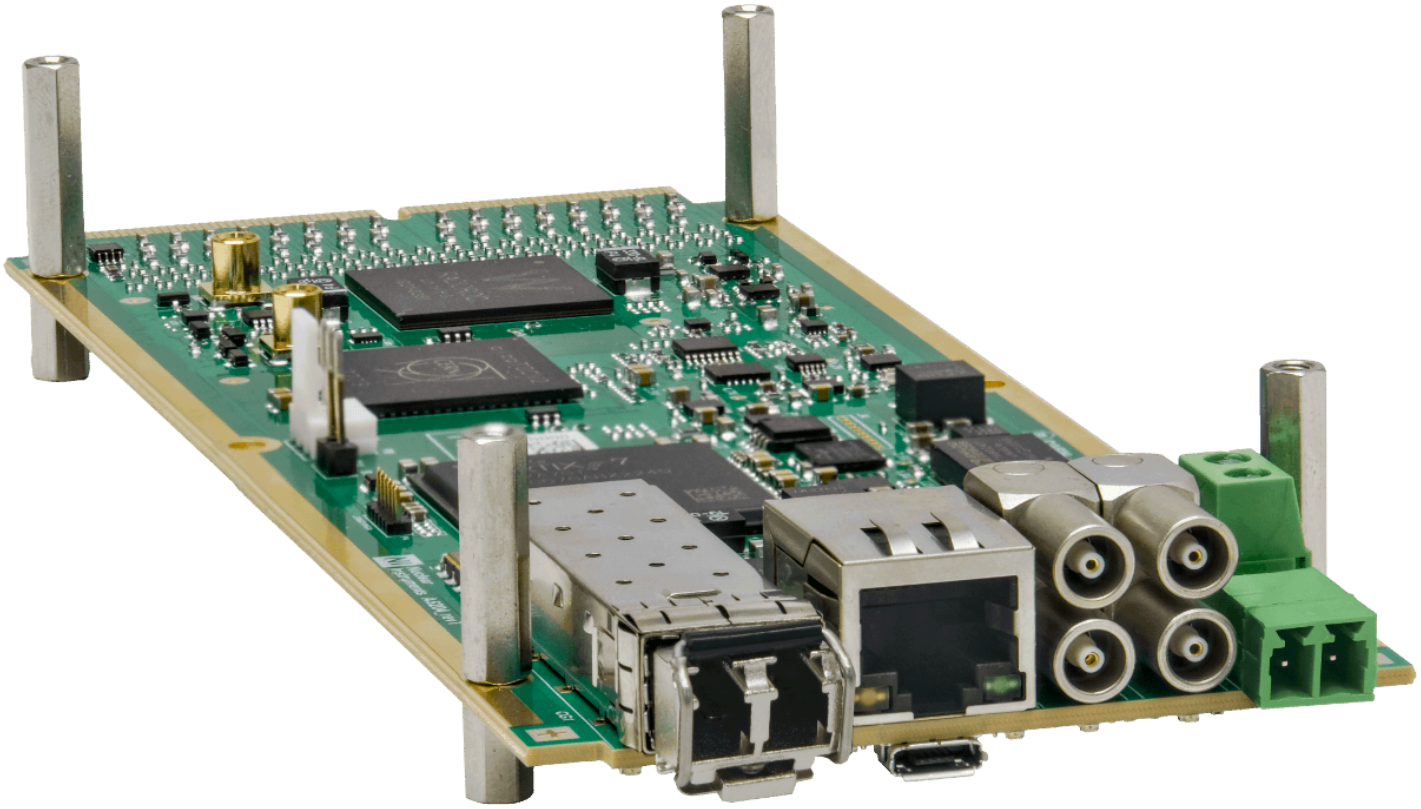
CAEN CODE: A5205

https://www.caen.it/products/A5205

Features



- 64-channel readout with Weeroc Psiroc ASIC
- Triggering down to 0.5 fC for sub-20 pF detectors
- Dual-gain charge measurement and ToT output
- Sub-ns timing resolution with picoTDC (3.125 ps LSB)
- Positive/negative input polarity supported
- Adjustable gain up to 4 V/pC, shaping from 20 ns to 3 µs
- Low dead time acquisition without multiplexed ADC
- Fully supported by Janus 5205 software suite

Description

The module **A5205** is a detector readout board suited for PIN diodes, silicon strips and GEMs, handling detector capacitances ranging from 0 up to few hundreds of pF. The module is part of the **FERS-5200 family**, a Front-End Readout System designed for the readout of large detector arrays such as SiPMs, multi-anode PMTs, Silicon Strip detectors, Wire Chambers, GEM, Gas Tubes and others. FERS is a distributed and scalable system, where each unit is a small card that houses 64 or 128 channels. It features a detector specific Front-End interfaced to a common infrastructure that guarantees readout interfaces, slow control and synchronization. Typically, the front-end is based on ASIC chips that allow for high density, cost effective integration of multi-channel readout electronics into small size and low power modules. FERS is a flexible platform: combining the same back-end (i.e. readout architecture and interface) with different types of front-end to fit a wide range of detectors.

The front end electronics of the **A5205** (and **DT5205**, which is the boxed version for desktop use) is based on the **Psiroc** chip (produced by Weeroc), that includes a Charge Sensitive Preamplifier (CSP), followed by 2 slow shapers (high and low gain) for the peak sensing ADC and 1 fast shaper for the discriminators that provide triggers and timing information. The individual channel triggers are connected to the FPGA, for hit counting and for triggering, and to a **picoTDC**, an ASIC chip produced by CERN, implementing a 64 channel TDC with LSB = 12.5 ps, for very precise timing measurements. Time Over Threshold (ToT) can also be used to estimate the pulse height, making it possible to acquire time stamp and PHA with very low dead time and extremely high rate, without the need of the multiplexed A/D conversion.

The most relevant **A5205** acquisition modes are:

- **Spectroscopy Mode**: in this mode, the acquisition is simultaneous for the 64 channels of the board. The analog chain made of pre-amplifier (both High and Low gain), shaper and peak sensing is used to acquire the PHA with high energy resolution and wide dynamic range. The common trigger, that initiates the A/D conversion through the multiplexed outputs, can be generated by a combination of the channel self-triggers or from an external signal received from the T0 or T1 inputs. In parallel to the ADC data for the PHA, it is also possible to get high resolution timing information from the picoTDC that receives the individual channel triggers. The event data packet is therefore composed by the common trigger time stamp, trigger ID, dual PHA information (High and Low gains, optionally zero suppressed), individual arrival time of the channel hits that fall in the acquisition window open by the trigger. In spectroscopy mode, after each trigger, there is a dead-time due to the multiplexed A/D conversion. The amount of dead-time is of the order of 30 us, although it depends on the configuration.
- **Counting Mode**: the purpose of this acquisition mode is to count the number of self-triggers (i.e. input pulses) of each channel in a time window of programmable size (dwell time). The internal memory buffers allow for saving the channel counts of consecutive time windows, thus implementing a Multi Channel Scaler (MCS) with 64 inputs. The counting mode can also be used to generate the trigger efficiency curves (i.e. counts as a function of the trigger threshold). Looking at these curves, it is possible to define the “zero” of the signal (offset), the minimum threshold above the noise as well as the size of the DAC LSB reported to the input range of the signal.
- **Timing Mode**: in timing mode, the peak ADC is disabled and the readout data are only those ones coming from the picoTDC. It is possible to acquire the ToA (Time of Arrival) and/or the ToT (Time over Threshold) of the input pulses. In timing mode, there is no dead-time due to the A/D conversion and there is no need of a common trigger, since the 64 channels are independent and can acquire data in streaming mode, just using their self-triggers (trigger-less acquisition). The ToT can be used to estimate the pulse charge with 1% linearity energy measurement up to 100 pC.
  The timing mode has 2 different options:
  - **Trigger Matching:** in this mode, there is a trigger signal that defines an acquisition window with arbitrary width and position with respect to the trigger. Only the hits belonging to that window will be recorded. Multiple hits on the same channels will be recorded, as far as there is space in the memory buffers. The acquisition trigger
    can be a combination of the channel self-triggers or an external signal connected to the T0/T1 inputs.
  - **Streaming Timing Mode:** this acquisition mode implements a continuous hit recording, without any gate or trigger windowing. All hits received by the inputs are time stamped (56 bit) and saved in the form of a sorted list, along with ToT if enabled.

Ordering Options

Code	Description	
WA5205XAAAAA	A5205 - 64 channel Psiroc unit for FERS-5200 with picoTDC	RoHS

Related Products

CAEN FERSlib Library

High level library for FERS-5200 Boards

DT5216

DT5215

Concentrator Board for FERS-5200

JANUS

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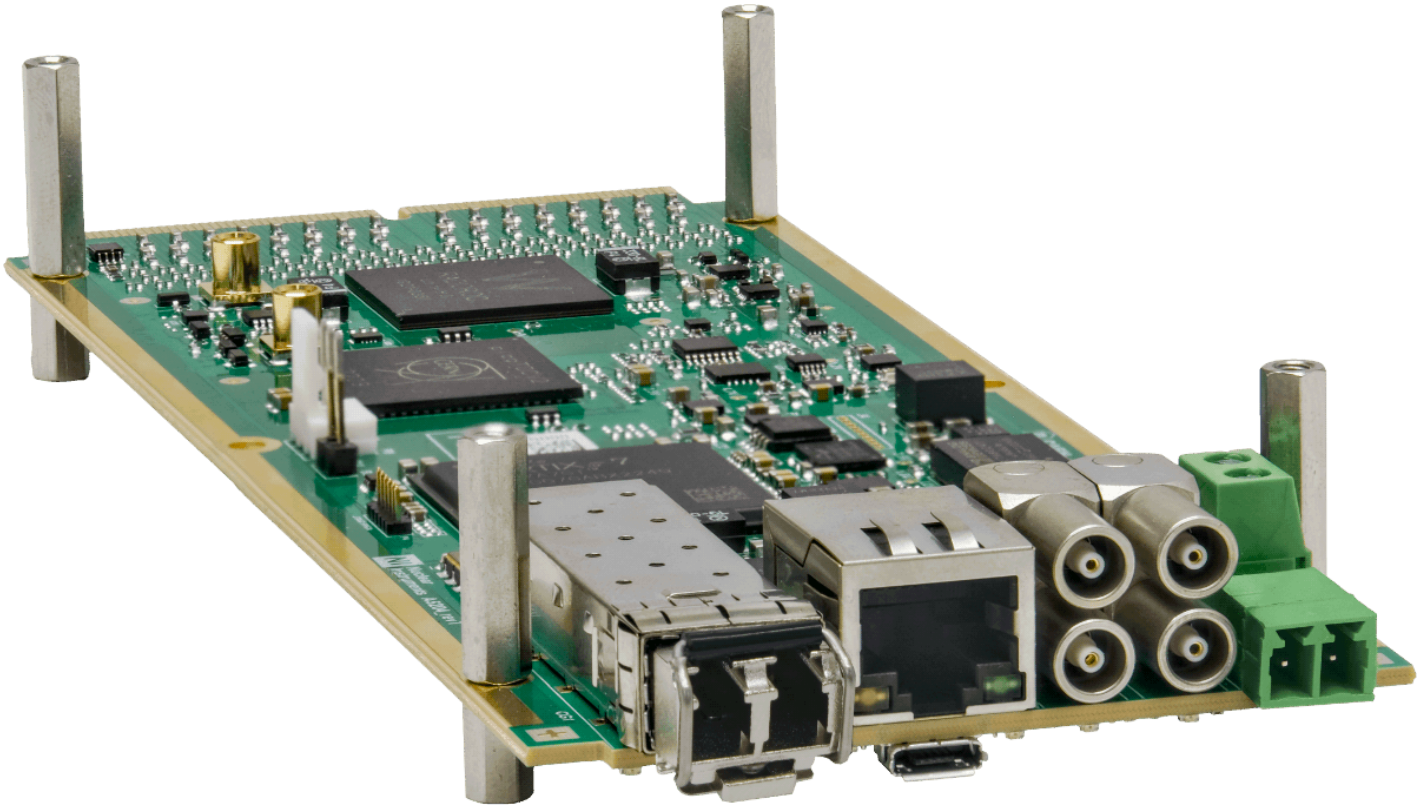
FERS-5200 DAQ SOFTWARE

DT5205

64 Channel Psiroc Desktop Unit for FERS-5200

Gallery



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