C205

32 Channel Charge Integrating ADC

Features

- Two simultaneous ranges: 120 and 900 pC
- 25 fC LSB
- 12-bit resolution (15 bit total dynamic range)
- 1.6 ms / 32 ch conversion time
- Integral non linearity: ±6.5 counts (low range); ±2.5 counts (high range)
- Gate width: from 100 ns to 5 µs
- Noise: ±1 count
- 2% interchannel uniformity
- 300 ns recovery after Fast Clear
- Positive, negative or differential input signals

Description

The **Mod. C205** is a single width CAMAC unit housing 32 charge integrating ADC channels. For each channel, the input charge, received when the GATE signal is active, is converted to a voltage level through a **Charge to Voltage Converter** (CVC); each CVC output voltage is then amplified by both a 1X-gain amplifier and a 7.5X-gain amplifier, and sequentially transformed into two corresponding 12-bit words through two parallel 12-bit Analog to Digital Converters (ADC): this allows to achieve a 15 bit total dynamic range. Meanwhile, a BUSY output signal is available at the corresponding pins of the 10-pin front panel connector. Each couple of words corresponding to a conversion value is stored into a RAM-type internal memory (readable via CAMAC) in sequential order.
At the end of the analog-to-digital conversion of the last input signal, a LAM signal is generated. At this point the conversion values corresponding to each input charge can be read via CAMAC.
The TEST input connector allows the user to perform test operation by using a single input signal common for all channels.

Technical Specifications

Packaging

1-unit wide Camac module

Inputs

DC coupled, 50 Ohm impedance for positive or negative input signals; 110 Ohm for differential input signals

Full scale

- 120 pC (15 bit)
- 900 pC (12 bit)

Conversion gain

31 counts/pC (15 bit), 4 counts/pC (12 bit)

Conversion time

1.6 ms/32-ch

Gain dispersion

± 2 counts MAX

Input offset voltage

± 2 mV

Integral non linearity

within ± 6.5 counts (15 bit), ± 1.6 counts (12 bit)

GATE width

100 ns to 5 µs

GATE timing

The GATE signal must precede the analog input by > 65 ns

TEST input sensitivity

about 30 times less than a channel

Pedestal/GATE width coefficient

- 50 counts/100 ns (15 bits), 7 counts/100 ns (12 bits) typical
- total pedestal: 350 counts (15 bits), 50 counts (12 bits) typical

Related Products

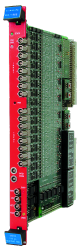
V792N

16 Channel Multievent QDC

C1205

16 Channel QDC

V965



16 Channel Dual Range Multievent QDC

C205

32 Channel Charge Integrating ADC

Gallery

This document, or parts thereof, may not be reproduced in any form or by any means without written permission from Caen S.p.A. Although every effort has been made to ensure the accuracy of information presented in this catalog, Caen S.p.A reserves the right to modify its products specifications without giving any notice; for up to date information please visit www.caen.it © Caen S.p.A - 2024

CAEN S.p.A.
Via Vetraia 11
55049 - Viareggio
Italy
Phone +39.0584.388.398
Fax +39.0584.388.959
info@caen.it
www.caen.it

CAEN GmbH
Brunnenweg 9
64331 Weiterstadt, Germany
Phone +49 (0)212.254.4077
Mobile +49 (0)151.16.548.484
info@caen-de.com
www.caen-de.com

CAEN Technologies, Inc.
1 Edgewater Street - Suite 101
Staten Island, NY 10305
USA
Phone +1.718.981.0401
Fax +1.718.556.9185
info@caentechnologies.com
www.caentechnologies.com

CAENspa India Private Limited
B205, BLDG42, B Wing,
Azad Nagar Sangam CHS,
Mhada Layout, Azad Nagar, Andheri West
Mumbai, Maharashtra 400053, India
info@caen-india.in
www.caen-india.in