

DT5550

32 Channel Programmable Readout System



Features



- 32-channel Sequencer and Readout System (fully differential inputs)
- Integrated system for managing digital and analog ASIC outputs
- Ideally suited for **R&D projects** involving ASICs with multi-channel detectors
- 48 differential digital lines and 2A power supply to support ASICs readout
- Multi-board support for system-building
- Optional Digitizer functionality via **DT5550AFE** (single-ended analog inputs) accessory
- 80MS/s, 14bit ADC
- USB 3.0 for fast data transfer
- "Open-FPGA Capability" via **Sci-Compiler software**, a graphical development platform for quick, user-friendly FPGA programming
 - Dramatically simplifies development of complex logic schematics and processing algorithms
 - Automatic VHDL firmware code generation via GUI-based block diagrams
 - Supports processing functions such as PHA-based Trapezoidal Filter, Peak Stretcher, Charge Integration, Waveform Recording, MCA, Scaler, and more...
- 8 programmable digital I/O on LEMO connectors for external control signals (trigger, veto, busy, etc...)
- Standard VHDCI Connectors
 - 1 analog connector with 32 analog channels and an I2C bus
 - 2 digital connectors carrying 24 differential digital lines (each) and programmable power supply for ASICs control"

Description

The CAEN **Mod. DT5550** is a **Programmable 32-channel Sequencer and Readout System** for physics application. It is one of the CAEN programmable board compatible with **SCI-Compiler**, the innovative software tool for **easy FPGA programming**, designed to help users in building a customized DAQ. The default firmware, the demo readout software and some design files are distributed for free and open source, allowing the user to minimize the effort in designing the DAQ.

The DT5550 is capable to manage simultaneously a large number of **digital** and **differential analog** signals, making it suitable to **readout most of the ASICs commonly used in physics applications**.

The DT5550 is fully supported by SCI-Compiler, a Windows-based graphical development system for **block-diagram-based FPGA programming**. This tool allows to develop and compile the firmware code using graphical blocks which represents the functionalities needed for firmware implementation (for example oscilloscope, TDC, MCA, charge integration, etc). SCI-Compiler automatically generates the VHDL firmware code starting only from logic blocks and virtual instruments that can be connected together in the GUI and, moreover, it generates C/C++/C#/Python Libraries for custom software development in Windows and Linux.

A complete, ready to use default firmware is provided for free and open source. The default firmware manages the basic waveform digitization and charge integration and it is preloaded on the board. The user can open the default firmware in SCI-Compiler and modify it in order to customize, for example, the trigger logic, the data online processing or integrate it in a larger system.

The SCI-Compiler license and one-year free upgrade is included with the DT5550.

The **SCI-55x0 Readout Software** is the free and open source Windows-based software developed to perform basic acquisitions with the DT5550. It works in conjunction with the DT5550 default firmware and it can be modified by the user according to the custom functions implemented in the firmware and for any other need.

Available board models and accessories are listed in the tab "ordering option" and "accessories".
Developed in collaboration with Nuclear Instruments.

Technical Specifications

Packaging

163 x 50 x 226 mm³ (WxHxD) Desktop

Analog Input

Channels: 32 Channels, Differential

Connector: VHDCI

Bandwidth: 31 MHz

Impedance: Zdiff = 100 Ω

Full Scale Range: 2 Vpp

Digital Input

Channels: 2 x 24 channels, Differential

Connector: 2 x VHDCI

Signal Type: CMOS 3.3V, LVCMOS 1.8V, LVDS, BLVDS

Impedance: Zdiff = 100 Ω

Coupling: AC

Digital Conversion

Resolution: 14 bits

Sampling Rate: 80 MS/s Simultaneously on each channel

Clock Generation

Clock source: internal/external

On-board programmable PLL provides generation of the main board clocks from an internal (25 MHz local Oscillator) or external (rear panel CLK-IN connector) reference

LEMO Digital I/O

CLOCK-IN (LEMO)

Zin = 50 Ω

Single-ended, 25 MHz, 3.3V

CLOCK-OUT (LEMO)

Rt = 50 Ω

Single-ended, 25 MHz, 3.3V, 50mA

GPIO 1 - 8 (LEMO)

General purpose programmable digital I/Os

Single-ended, Zin / Rt = 50 Ω

Memory

16 kS/ch

Trigger

Trigger Source

Internal/External: managed by the default firmware
Complex trigger logic: implementable by the user on the open FPGA

Trigger Propagation

Through programmable LEMO GPIO 1 - 8

Trigger Time Stamp

Default FW: 32-bit counter, 12.5 ns resolution, 50 s range;
Custom FW: defined by the firmware design

Synchronization

Clock Propagation

LEMO CLOCK IN/OUT connectors

Acquisition Synchronization

Through programmable LEMO GPIO 1 - 8

FPGA

Open FPGA

Xilinx XC7K160T (Kintex-7 family)

Communication Interface

USB 3.0

USB 2.0 back compatibility Up to 240 MB/s transfer rate

Firmware

Default: Waveform recording and Charge Integration

Custom: Use SCI-Compiler to develop your own firmware (LICENSE INCLUDED)

Firmware Upgrade

Firmware can be upgraded via USB 3.0 or mini-USB debugger (on-fly)

Software

- SCI-5550 Readout Software to manage the default firmware
- SCI-Compiler for custom firmware development

Ordering Options

Code	Description
WDT5550XAAA	DT5550 - 32 Channel DAQ System with Programmable FPGA and Sequencer RoHS

Accessories

DT5550AFE



Single Ended to Differential Input Adapter for DT5550

Related Software

CAEN Toolbox



Multi-Functional Software Suite for the Upgrade of Front-end Boards, Bridges and Power Supplies

Related Products

DT5550AFE



Single Ended to Differential Input Adapter for DT5550

Gallery



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