

New

DT5560SE

**32 Channel 14 bit
125 MS/s Open
FPGA Digitizer**



Features



- 32 channels, 14-bit @125 MS/s Digitizer
- Handy **Desktop** form factor
- Based on powerful Xilinx Zynq-7000 SoC with **open FPGA**
- Fully supported by **SCI-Compiler** for easy FPGA programming (Firmware runtime license included onboard)
- Ideally suited to readout **PMTs and Position Sensitive detectors** in **R&D/Lab development** stage
- **32 Single-ended** analog inputs on LEMO connectors
- **Programmable analog frontend**
- **[x1:x100] analog gain**, adapting to many HEP and nuclear spectroscopy detectors
- Board-to-board **synchronization** with a single CAT5e cable.
- Configurable digital I/Os to interface with external systems
- Maximum **flexibility**: USB2.0, Ethernet, and Optical Link (OPTIONAL) connectivity, to support remote management as well as extreme fast data flow
- **2.4" touch screen display** for quick configuration and status control
- **Web Interface** for quick board start-up
- Default firmware for trapezoidal filter PHA and waveform recording
- Open-source Open Hardware Readout Software

Description

The CAEN Mod.**DT5560SE** is a Desktop, 32 Channel, 14-bit 125MS/s Waveform Digitizer which features an **Open FPGA** format which offers the user vast programmable data processing capabilities.

The DT5560SE Open FPGA Digitizer is ideally suited to readout detectors commonly used in HEP and nuclear spectroscopy, exploiting the handy form factor for R&D and prototyping in a laboratory. By taking advantage of the powerful SoC architecture the user can quickly and easily design **custom logic and pulse processing algorithms** on the open FPGA, as well as develop middleware/software which perfectly matches of the application of interest. No expertise in VHDL/Verilog is required for the user to utilize this powerful tool.

The board can simultaneously manage **digital** (LVDS, NIM, TTL) and **analog** signals, thus supporting the implementation of a wide range of functionalities required by physics experiments: Signal Digitization, Complex Trigger Logic, Pulse Height Analysis with MCA capabilities, Time Tagging, Pulse Shape Discrimination, etc. The DT5560 features single-ended analog inputs on LEMO connectors and an advanced programmable input stage with different possible gain and offset, suitable to adapt to a wide range of detectors.

Critical to the DT5560SE design is an **open-FPGA** architecture. Thanks to **SCI-Compiler** software, users can combine several processing blocks in a block diagram, supporting the quick and simple development of firmware algorithms critical to data processing. In few clicks, and without the knowledge of any FPGA programming language, it is possible to implement **Pulse Height Analysis (PHA)**, highly accurate event timing and timestamping (TDC), mathematical operations (including data fitting), Pulse shape discrimination (PSD), and much more.

Free and open-source **SCI-55x0 readout software** is also provided. This open-source demo software is designed to manage the standard pulse height analysis firmware implementing energy measurements using a trapezoidal filter together with waveform recording.

Developed in collaboration with Nuclear Instruments.

Technical Specifications

General

Form Factor: Desktop 257 x 102 x 331 mm³ (WxHxD)

Analog Input

Channels: 32 single-ended inputs on LEMO

Impedance: 50 Ω /1 k Ω programmable

Bandwidth: 60 MHz, Programmable DC offset adjustment on each input in the full scale range

Analog Coarse Gain: [x1:x100]

Full Scale Range: [0.015 V_{pp}: 1.5 V_{pp}]

Digital I/Os

USER IO 0...2 (LEMO)

- Programmable Digital I/Os, function stated at firmware level.
- Can be used as Trigger, Start, Busy
- Single-ended, Z_{in} / R_t = 50 Ω

Digital Conversion

- Resolution: 14 bits
- Sampling Rate: 125 MS/s Simultaneously on each channel

Clock Generation

125 MHz ADC clock

Clock sources: internal/external

Internal 25 MHz oscillator

External 25 MHz – USER IN 0 or SYNC connector

Trigger

	Trigger Source	Trigger Time Stamp
Trigger Propagation		
<ul style="list-style-type: none">• Through USER I/Os and Sync Connector	<ul style="list-style-type: none">• Internal/External: managed by the default firmware• Complex trigger logic: implementable by the user on the open FPGA	<ul style="list-style-type: none">• Default FW: 32-bit counter, 8 ns resolution, 26-day range• Custom FW: defined by the firmware design

Synchronization

Clock Propagation: USER I/Os connectors SYNC Connector

Acquisition Synchronization

- Through programmable LEMO
- Through dedicated SYNC Connector

Sync connector allows to cascade multiple units and synchronize them with a single standard CAT5e cable

FPGA

Open FPGA: Xilinx Zynq-7000 SoC Z-7030

Memory

- 1 GByte of memory for list readout on each SoC
- Up to 8kS/ch for simultaneous waveform readout

Communication Interface

The different readout interface allows to integrate the DT5560SE in existing experimental environment.

Ethernet

1 Gbps

USB2.0

1x mini-USB

Optical Link

- Slots for 2 x 10 Gbps SFP + transceivers
- (communication protocol not implemented by default)

Firmware

Default

- Waveform recording and Pulse Height Analysis
- Ethernet/USB communication

Custom

- Use SCI-Compiler to develop your own firmware

Firmware Upgrade

Firmware can be upgraded via Ethernet, mini-USB or JTAG mini-USB debugger (on-the-fly)

Software

- SCI-55X0 Readout Software to manage the default firmware
- SCI-Compiler for custom firmware development

Power Requirements

- Voltage: 100-240 Vac
- Frequency: 50/60 Hz
- Typ. power consumption: 300 mA @ 220 Vac

Ordering Options

Code	Description
WDT5560SEXAA	DT5560S 32 Ch. 14 bit 125 MS/s Digitizer single-ended RoHS

Related Software

Sci-Compiler



Graphical Programming Language for CAEN Open FPGA Boards

Related Products

R5560



128 Channel 14 bit 125 MS/s Open FPGA Digitizer

R5560SE



128 Channel 14 bit 125 MS/s Open FPGA Digitizer

Gallery



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