CAEN
Tools for Discovery

Discontinued

DT5702

32 Channel SiPM Readout Board for Cosmic Rays Veto BOXED

Features

- Readout board for SiPM, tailored for **Cosmic Rays Veto** systems in Neutrino experiments.
- Based on **32-channels** WeeROC CITIROC ASIC
- **Coincidence** of signals from each pair of adjacent even-odd channels
- Provides bias voltage in the range of 20-90 V, individually adjustable for each of 32 SiPMs
- Amplification and shaping of the SiPMs output pulse on each of 32 channels
- Discrimination of shaped signal at configurable level from 0 to 50 SiPMs photo-electrons
- Timing resolution down to 1 ns with stable external reference signals
- Readout via 100 Mbps Ethernet, double ports for multiboard daisy-chain
- ROOT-based readout software

Description

The **CAEN Mod. DT5702** is the desktop version of the **A1702**. It is a custom design developed by the Albert Einstein Center for Fundamental Physics of the University of Bern for the readout of SiPM arrays used in the Cosmic Rays veto of Liquid Argon Neutrino Experiments. The board is designed for the exact purpose of detecting coincidences at the far ends of scintillating fibers coupled with SiPMs and measure the signal energy as well as the time of arrival for track reconstruction.

The analog input signal is processed by CITIROC, a **32**-channel ASIC from WeeROC. Each channel is made of a high-gain charge preamplifier (x 10 – x 600 gain range), fast shaping with the peaking time of **15 ns** and slow shaping with configurable shaping time in the range of **12.5 ns** to **87.5 ns**. Signals from the fast shapers are discriminated (programmable threshold) and produce digital signals (T0-T31) for event triggering. These signals are then combined in the FPGA to give coincidence triggers. The input signals height can be stored in the ASIC Sample-and-Hold (S/H) circuit and multiplexed to a single analog output. This output is routed to an external ADC for sampling and energy list decoding.

The board allows to perform timing measurements, thanks to external reference signals to be fed at the dedicated LEMO inputs. Using very stable signals, like PPS pulses, it is possible to reach timing resolution down to 1 ns. Additional T-IN/T-OUT connectors for board-to-board trigger validation are also available.

The board communicates with the host computer through Ethernet protocol, relying on a ROOT-based demo software running on Linux.

Technical Specifications

Mechanical

Desktop Dimension
218 W x 20 H x 63 L mm^3 (without connectors)
230 W x 20 H x 80 L mm^3 (including connectors)

Power Consumption

0.550 A @ 5 V

Analog input

Channels: 32 channels, based on Weeroc CITIROC

Connectors: 72-pin, 2-row, 2.54 mm header strip

Bias Voltage

Common Bias: from 20 V to 90 V
- 8-bits DACs for individual fine adjustment: +0.5 V to +4.5 V

Charge Amplifier

Configurable gain x10 - x600

Shaper

- Fast shaping: shaping time of 15 ns
- Slow shaping: configurable shaping time in the range of 12.5 ns to 87.5 ns

Discriminator

from 0 to 50 SiPM photoelectrons
- 10-bit DAC common threshold
- 4-bits DAC for fine adjustment of individual channels

TDC

250 MHz clock frequency - 4 ns resolution

Time Stamp

down to 1 ns resolution

*achievable only using stable external reference signal

Digital Conversion

Resolution: 12-bit

Digital I/O

- **TIN** (LEMO)
  Validation input
- **T0** and **T1** (LEMO)
  Reference Inputs for Timing
  3.3V LVCMOS, High Impedance
- **TOUT** (LEMO)
  Output pulse
  3.3V LVCMOS

Trigger

Internal Trigger: **OR32** mode or **channel pairs** coincidences
Validation trigger: Only the events that falls inside the validation windows given at TIN are considered valid.

Memory buffer

up to 1024 events

Multi Boards Connection

Daisy-chaining of up to 256 units into one network interface.

Communication Interface

100 Mbps Ethernet links

Software

User interface is a demo CERN ROOT script running on Linux

*tested with ROOT 6.10/02 on Ubuntu 16.04 OS - 64 bit

Ordering Options

Code	Description	
WDT5702XAAAA	DT5702 - 32 Channel SiPM readout Front-End Board BOXED (Discontinued)	RoHS

Related Products

DT5215

Concentrator Board for FERS-5200

A5202

64 Channel Citiroc unit for FERS-5200

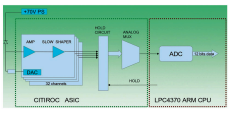
DT5202

Desktop 64 Channel Citiroc unit for FERS-5200

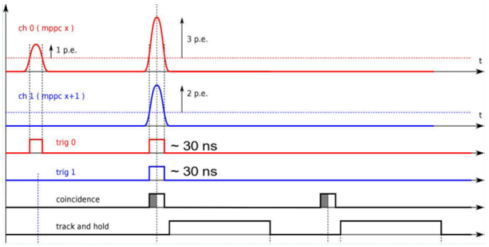
A1702

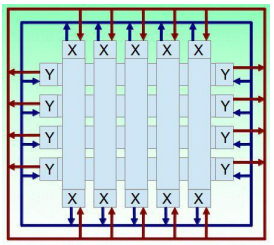
32 Channel SiPM Readout Board for Cosmic Rays Veto

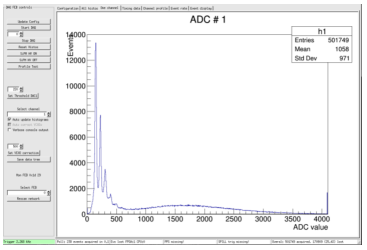
Gallery

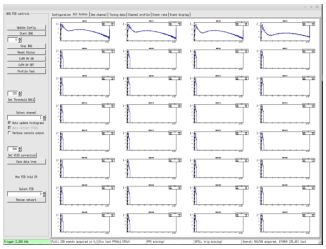


Block-scheme of analog signal processing circuit.









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