1 System Overview

FERS-5200 is a Front-End Readout System designed for the readout of large detector arrays such as SiPMs, multi-anode PMTs, Silicon Strip detectors, Wire Chambers, GEM, Gas Tubes and others. FERS is a distributed and scalable system, where each unit is a small card that houses 64 or 128 channels. It features a detector specific Front-End interfaced to a common infrastructure that guarantees readout interfaces, slow control and synchronization. Typically, the front-end is based on ASIC chips that allow for high density, cost effective integration of multi-channel readout electronics into small size and low power modules. FERS is a flexible platform: combining the same back-end (i.e. readout architecture and interface) with different types of front-end to fit a wide range of detectors.

The **A5204** (and **DT5204**, which is the boxed version for desktop use) is a member of the FERS-5200 family. It uses the **Radioroc** chip (produced by Weeroc) for the readout of SiPM detectors. Radioroc allows triggering down to 1/3 p.e. and provides dual-gain energy measurement with excellent Signal-to-Noise Ratio on the high gain (SNR over 10 for single p.e.) and large dynamic range on the low gain. Thanks to the programmable shaping time, that can be different for low and high gain, the Radioroc can perform Pulse Shape Discrimination with organic and inorganic scintillators coupled to SiPMs.

The A5204 includes a High Voltage generator (up to +80V, 10 mA) for the SiPM biasing; a channel-by-channel 8-bit DAC contained in the Radioroc ASIC allows for fine adjustment of the SiPM bias voltage and SiPM gains homogenization. Besides the slow shaper + peak sensing chain for the acquisition in spectroscopy mode, Radioroc includes configurable fast pre-amplifiers followed by discriminators that can output 64 individual channel triggers with jitter as low as 55 ps FWHM on a single p.e. The individual channel triggers are connected to the FPGA, for photo-counting up to 200 MHz as well as for the implementation of coincidences, majority and topological acquisition triggers. The individual triggers are also connected to a **picoTDC**, an ASIC chip produced by CERN, implementing a 64 channel TDC with LSB = 3.125 ps, for very precise timing measurements. Time Over Threshold (ToT) can also be used to estimate the pulse height, making it possible to acquire time stamp and PHA with very low dead time and extremely high rate, without the need of the multiplexed A/D conversion.

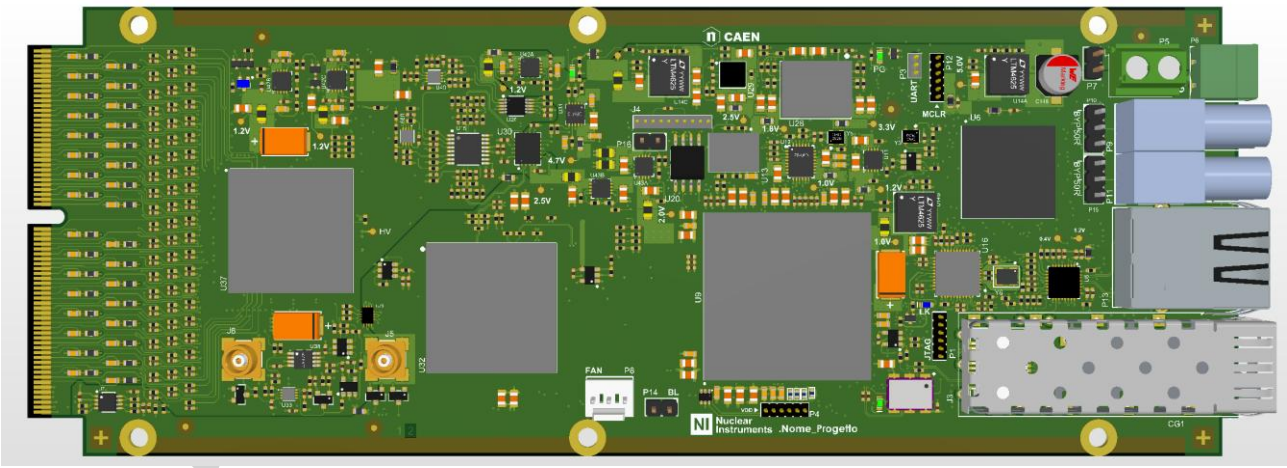

Fig. 1.1: FERS-A5204: board rendering

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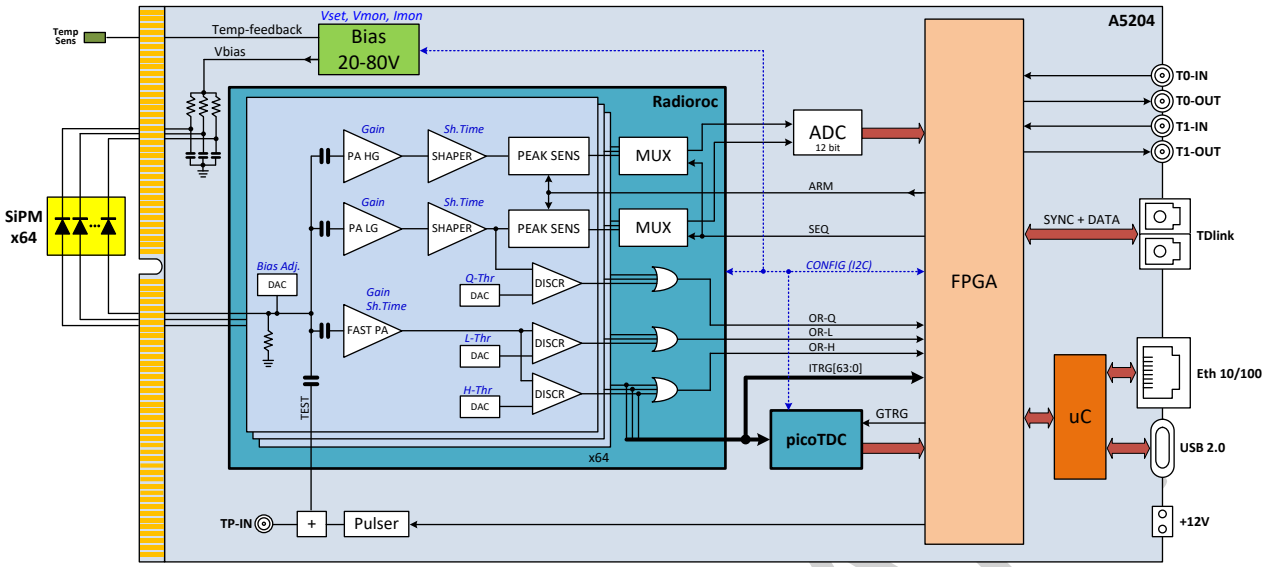

Fig. 1.2: Simplified block diagram

For small setups a single A5204 unit can be used stand alone, without any additional hardware, by simply connecting the unit to a PC via USB 2.0 or Ethernet 10/100T. For large readout systems, a flexible and scalable network of units can be created by means of the high speed optical link called **TDlink**. The TDlink system supports up to 128 FERS units to be connected to and managed by one **DT5215** FERS Data Concentrator Module. The TDlink supports optical daisy chaining and provides slow control, high speed data readout, synchronization between the units (clock and sync distribution), as well as command broadcasting for triggers, time resets, etc.

Fig. 1.3: DT5215: 8 link Data Concentrator

The A5204 is fully supported by the CAEN **Janus** open source software for Windows® and Linux. Janus can run in console mode (C program, without graphics) or connected to a GUI written in Python. The GUI has configuration panels and run control which make it easy to manage acquisition. Both console and GUI modes acquire data from multiple boards, manage configuration, event building, PHA and timing histograms (deltaT and/or ToT), display data statistics (hit rate, throughput, etc…), plot histograms, and save output, including spectra and list files with the acquired timing data.

2 Acquisition Modes

The A5204 supports the following acquisition modes:

Spectroscopy Mode: in this mode, the acquisition is simultaneous for the 64 channels of the board. The analog chain made of pre-amplifier (both High and Low gain), shaper and peak sensing is used to acquire the PHA with high energy

resolution and wide dynamic range. The common trigger, that initiates the A/D conversion through the multiplexed outputs, can be generated by a combination of the channel self-triggers or from an external signal received from the T0 or T1 inputs. In parallel to the ADC data for the PHA, it is also possible to get high resolution timing information from the picoTDC that receives the individual channel triggers. The event data packet is therefore composed by the common trigger time stamp, trigger ID, dual PHA information (High and Low gains, optionally zero suppressed), individual arrival time of the channel hits that fall in the acquisition window open by the trigger. In spectroscopy mode, after each trigger, there is a dead-time due to the multiplexed A/D conversion. The amount of dead-time is of the order of 10 us, although it depends on the configuration.

Counting Mode: the purpose of this acquisition mode is to count the number of self-triggers (i.e. input pulses) of each channel in a given time window (dwell time). Thanks to the ability of the Radioroc to trigger down to 1/3 p.e., the A5204 is an ideal solution for the applications that require single photon counting. The internal memory buffers allow for saving the channel counts of consecutive time windows, thus implementing a Multi Channel Scaler (MCS) with 64 inputs. Channel pairing for coincidence counting is also available. The counting mode is often used in SiPM characterization, to measure the DCR as well as to find the "staircase" curves, that is the variation of the counting as a function of the trigger threshold. There is a specific option in the Janus software to acquire and plot the SiPM staircase curves.

Timing Mode: in timing mode, the readout data are only coming from the timing information of the channel self-triggers read by the picoTDC. It is possible to acquire the ToA (Time of Arrival) and/or the ToT (Time over Threshold). Since the peak sensing chain read by the ADC is not used, there is no dead-time due to the A/D conversion. In timing mode, the channels are independent and there is no need to have a simultaneous acquisition controlled by a common trigger. The ToT can be used to estimate the pulse charge (PHA) with 1% linearity energy measurement up to 2000 p.e. If needed, a common time reference signal can be used to open an acquisition gate and to calculate deltaT timing between the channel triggers and the common Tref signal. *NOTE: the picoTDC has 64 channels that are all used for the self-triggers, therefore the timing of the Tref signal is acquired at lower resolution (~100 ps?)*

The timing mode has 4 different options:

- **Common Start:** there is a common start signal (connected to T0 or T1 input) that opens the acquisition gate and represents the time reference. The gate width is programmable by software. The event data contain the **deltaT** time measurements ($\Delta T_N = T_N - T_{REF}$) as well as the ToT. Any hit falling outside the gate will be discarded. In the case of multiple hits in the same channel, only the first will be used.
- **Common Stop**: similar to common start, with the difference that the time reference is used as a stop that closes the acquisition gate ($\Delta T_N = T_{REF} - T_N$). In case of multiple hits, only the last one will be used. In common stop mode, it is possible to manage the cases where the acquisition trigger arrives with some delay (latency) and it is necessary to go back in time to find the events of interest. Indeed, the local memory buffers keep the recorded hits while waiting for a Tref that opens a retroactive gate. Hits oldest than the maximum "look back" window are automatically discarded from the memory buffers.
- **Trigger Matching**: in this mode, there is a trigger signal that defines an acquisition window with arbitrary width and position with respect to the trigger. Only the hits belonging to that window will be recorded. Multiple hits on the same channels will be recorded, as far as there is space in the memory buffers. The acquisition trigger can be a combination of the channel self-triggers or an external signal connected to the T0/T1 inputs.
- **Streaming Timing Mode**: this acquisition mode implements a continuous hit recording, without any gate or trigger windowing. All hits received by the inputs are time stamped (56 bit) and saved in the form of a sorted list, along with ToT if enabled.

3 Adapters and accessories

The A5204 has an input edge card connector, type **HSEC8-170**, which mates to a Samtec HSEC8-170-01-S-DV. The connector has 140 contacts (0.8 mm pitch) and brings the SiPM signals (64 anodes + 64 cathodes), a few control signals and a 3.3V power line. The edge connector makes it possible to build a custom backplane or a flange for the interconnection to the detectors. CAEN also offers a wide range of adapters and cables, in order to provide different connectors, as well as the ability to remotely operate the detectors.

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The DT5204 (desktop version of the A5204) embeds the adapter in the front panel of the module. The user can easily replace the panel with another version by simply removing four screws.

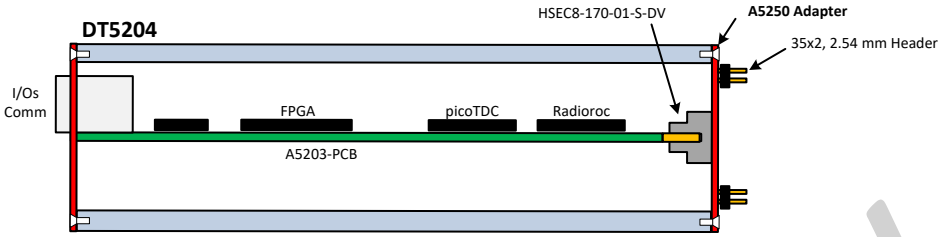

Fig. 3.1: DT5204 with A5250 adapter

Adapters:

A5250: this is a general-purpose adapter that simply brings the 140 contacts of the edge connector to two 35x2, 2.54 mm male header connectors.

A5251: adapter for Hamamatsu MPPC matrix S13361-3050AE-08 (1x1 inch). The matrix is plugged into two Samtec SS4-40-3.0-LDK-TR connectors. The adapter is equipped with a TMP37 temperature sensor for the bias auto adjust. Included with the adapter is a dark plastic box covering the matrix, with an FC connector for the fiber optic that can be connected to a LED driver such as the CAEN SP5601.

A5253: adapter to 64+1 individual 3 pin, AMPMODU type 3-102203-4 connectors (the 65th connector is for the remote temperature sensor). The connectors bring anode, cathode and ground signals and allow the SiPMs to be mounted separately. Individual ramotization cables are also available (tested up to 3 m).

A5254: adapter for OnSemi (ex SensL) SiPM matrix ARRAYJ-60035-64P-PCB and ARRAYC-60035-64P-PCB (2x2 inch). The matrix is plugged into two Samtec QSE−040−01−F−D−A connectors. Like the A5251, the adapter houses a temperature sensor and is provided with a dark plastic box covering the matrix.

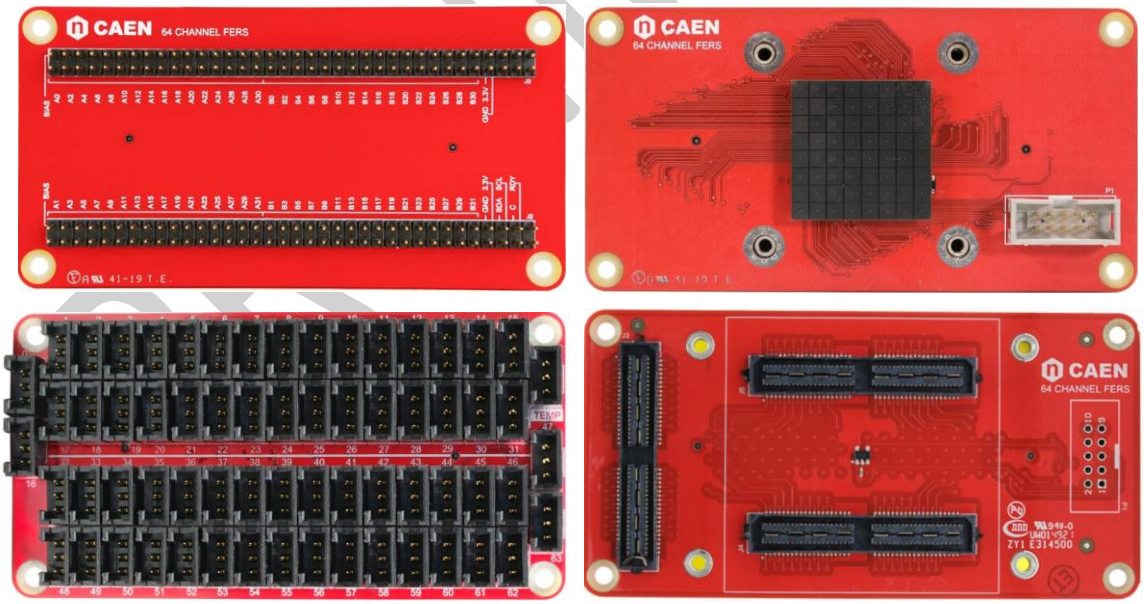

Fig. 3.2: A5250, A5251, A5253, A5254 Adapters (from top left to bottom right)

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Remotization cables:

A5260: micro-coaxial cable for HSEC8 edge connector remotization. Tested up to 3m without any significant signal degradation.

Fig. 3.3: FERS remotization cable

PRELIMINARY

A5204 Technical Specifications (prelim.)

MECHANICAL		**Dimensions** W = 74.0 mm; L = 198.7 mm; H = 22.0 mm **Weight** 165 g
INPUTS		64 channels Input edge connector type Samtec HSEC8-170. Mating connector: Samtec HSEC8-170-01-S-DV Signal polarity: Positive Each SiPM input has two pins: - Cathode with HV bias (min = +20V, max = +80V) - Anode closed to ~100 ohm, feeding the Radioroc inputs
HIGH VOLTAGE (SiPM Bias)		HV module for SiPM biasing (A7585D) HV Range: +20V/+80V, Max 10 mA Individual bias adjustment on channel basis (8 bit DACs, LSB = ~2 mV, adjust range = 550 mV) Automatic temperature feedback for SiPM gain stabilization
SPECTROSCOPY	**SENSITIVITY (GAIN)**	**High Gain**: Min = 5, Max = 80, 16 steps (1 step = 5) **Low Gain**: Min = 0.5, Max = 8, 16 steps (1 step = 0.5)
	SHAPING TIME	Short Range: Min = 20 ns, Max = 300 ns, 16 steps (1 step = 20 ns) Long Range: Min = 80 ns, Max = 1200 ns, 16 steps (1 step = 80 ns)
	DYNAMIC RANGE	Up to 2000 photo-electrons @ 10^6 SiPM gain
TIMING & COUNTING	**SELF-TRIGGERS**	Dedicated fast preamps + discriminator for SiPM pulse detection. Trigger down to 1/3 p.e. **Fast Preamp**: Gain: Min = 15 (BW = 480 MHz), Max = 100 (BW = 55 MHz), 32 steps **Discriminator**: Dual Threshold. Range = 278 mV; 1024 steps, 1 step = 0.27 mV
	TIMING RESOLUTION	55 ps FWHM on a single p.e. Time Stamp Range: 64 bit Intrinsic timing resolution of picoTDC = 3.125 ps LSB
	TOT	Time over Threshold (ToT): 1% linearity energy measurement up to 2000 p.e.

COUNTING	Photon counting up to 200 Mcps per channel MCS mode with programmable dwell time: from 16 ns to ~34 s
TRIGGER LOGIC	Global trigger common to 64 channels: used in Spectroscopy mode to start Peak acquisition, in Timing mode to generate the acquisition windows (Gate). Trigger-less acquisition only in Streaming mode. Global Trigger Sources: • OR of self-triggers = OR(0..63) • Plane coincidence: OR(0..31) AND OR(32..63) • Paired channels: AND(0..1) OR AND(2..3) … OR AND(62..63) • Majority with programmable threshold • External trigger (T0-IN, T1-IN, LEMO, TTL/NIM) • Internal periodic trigger with programmable frequency
SYNCHRONIZATION	Acquisition Trigger Time Stamp: 56 bit, step = 8 ns. Two synchronization modes: • T0 or T1 IN-OUT daisy chain: max jitter = 100 ns • fiber optic (TDlink) and DT5215 Concentrator: up to 128 boards, max jitter 50 ps
INPUT ADAPTERS	**A5250**: two 35x2, 2.54 mm male header connectors **A5251**: adapter for Hamamatsu MPPC S13361-3050AE-08 (two Samtec SS4-40-3.0-LDK-TR connectors) **A5253**: 64+1 individual 3 pin, AMPMODU type 3-102203-4 connectors **A5254**: adapter for OnSemi matrix ARRAYJ-60035-64P-PCB and ARRAYC-60035-64P-PCB (two Samtec QSE-040-01-F-D-A connectors) By default, the desktop version DT5204 comes with an A5250 as a front panel.
FRONT PANEL I/Os	**T0-IN**, **T1-IN**: LEMO-00 connector, NIM or TTL (terminated to 50 Ω) **T0-OUT, T1-OUT**: LEMO-00 connector, TTL (50 Ω termination required) SW selectable IN-OUT bypass and termination removal for daisy chaining **Functions** (SW programmable): Trigger, Acquisition Start/Stop, Sync, Busy, Veto, Signal inspection, etc…
FRONT PANEL LEDs	GREEN: Power-ON, Init-Done, Run, Trigger, Data Ready, T0-IN, T1-IN ORANGE: Event Overrun (rejected triggers because received while busy) RED: Failure (missing clock, over-temperature, etc…)
INTERNAL PULSER	Radioroc provides a test input pin that can be internally connected to the pre-amplifier inputs, channel by channel. The test signal can come from an external signal (MCX connector on the PCB) or generated by an internal pulser with programmable amplitude. The internal pulser can be trigger by T0/T1 IN or by the internal periodic trigger.
ACQUISITION MODES	**Spectroscopy:** The common trigger initiates the peak sensing detection and A/D conversion (12 bit) on all channels simultaneously. Conversion time = ~10 µs. Output Data: Trigger time stamp, Trigger ID, PHA (Low and/or High Gain). Zero suppression with programmable threshold. **Counting:** 32 bit counters, up to 200 MHz. Common trigger defines dwell time (i.e. counting window). No dead-time between subsequent windows. Internal period trigger from 16 ns to ~34 s. Output Data: Trigger time stamp, Trigger ID, channel counts. Zero suppression available. Counters are automatically reset after each trigger. **Timing (Common Start):** The Tref signal (T0, T1 inputs) is a common start that opens the acquisition gate with programmable width. Channel self-triggers are acquired as ΔT from Tref and, optionally, as ToT for PHA estimation. Output Data: Trigger (=Tref) time stamp, Trigger ID, ΔT or ΔT+ToT **Timing (Common Stop):** Same as common start, with Tref used as a common stop that closes the acquisition gate. Acquired events are those ones arrived before the trigger (look back acquisition). **Timing (Trigger Matching):** The common trigger signal defines an acquisition window with programmable width and offset. All hits falling into the window will be recorded. Multi-hit acquisition is supported. Output Data: Trigger time stamp, Trigger ID, ToA or ToA+ToT

	Timing (Streaming): continuous hit recording, without any gate or trigger windowing. All hit time measurements are expressed as 64 bit time stamps and saved in the form of a sorted list. Output Data: ToA or ToA+ToT
COMMUNICATION INTERFACES	**USB 2.0:** microUSB connector. Bandwidth = ~ 3 MB/s **Ethernet:** RJ-45, 10/100 Mbit/s. Bandwidth = ~ 2 MB/s **TDlink:** Optical link (~300 MB/s) with synch distribution. Allows for multi-board synchronization, slow control and data readout. Data Concentrator **DT5215** required.
POWER	power supply voltage: +12 V (min = +7V, max = +15V) power consumption: t.b.d. 110V/220V AC/DC converter provided with Desktop version only.
FIRMWARE	Firmware of FPGA be upgraded via USB or Ethernet Firmware of µC can be upgraded via Ethernet only
SOFTWARE	Open source **Janus** software for Windows® and Linux. Two operating modes: - console mode: C program with console commands and display (gnuplot for plots). Scriptable execution. - GUI mode: Python GUI for configuration and run control (C program running in background). **Janus features**: Multiple board acquisition with event building based on trigger ID or time stamp. PHA energy spectrum (Low and High Gain). ToT spectrum (represents PHA in timing mode) ΔT spectrum. Staircase curves (threshold scan) Live Display: channel hit count and rate, trigger rate, lost triggers, data throughput, acq. time, etc… Plots: PHA, ΔT, ToT, hit rate, 2-D heat map with channel hit rates or PHA. Output Files: histograms (spectra), list files (PHA, ToA, ToT, ΔT), Run Info, Sync file.

PRELIMINARY