N6741

32 Ch Peak Sensing ADC

Features

- 1-unit wide NIM Module
- 1k, 2k, 4k 8k, 16k Peak Sensing ADC
- 32 input channels, single-ended, with 68-pin ERNI SMC connector (Zin: 2.5 kΩ)
  - Accepts positive and negative inputs
  - 4 Vpp or 8 Vpp Full Scale Range software selectable (3.75 Vpp and 7.5 Vpp when sliding scale is enabled)
- Common Gate mode (32 channels converted at once) with linear gate width or programmable by software
- Low dead time (about 50 ns after the previous gate closes)
- Sliding scale algorithm for DNL reduction
- Zero suppression with programmable threshold
- Multi-Event Buffer (1024 events)
- USB2.0 and Optical link (CAEN CONET proprietary protocol) communication interfaces
- Windows and Linux drivers, C and LabVIEW libraries, demo software
- Firmware upgradable by the user

Description

The **N6741** is a **Digital Peak Sensing ADC** belonging to a new generation of detector readout systems based on a mixed analog-digital acquisition chain, combining a high channel density (**32 channels**) and a **low dead time**. The FLASH ADC architecture makes it possible to achieve an extremely low conversion time of the pulse peak, so new conversions take place less than 50 ns after the previous gates close.

Conversion gain ranges **from 1k up to 16k** channels with a low differential non-linearity (DNL) thanks to the *sliding scale method*.

Receiving the typical slow signal from a **Charge Sensitive Preamplifier** followed by a **Shaping Amplifier** (e.g. CAEN **N1068**), the FPGA identifies the peak of the pulse within a gate by means of digital filters. *The acquisition is common to all channels and takes place as soon as the GATE arrives.* The energy value together with the time of arrival of the event is first stored in a 1024 multi-event buffer and made available for the readout by USB or optical link interface (Daisy-chainable). Both the energy spectrum and the list of events is available through the software interface. Data throughput can be reduced by the Zero Suppression algorithm with a programmable threshold.

The front panel hosts LEMO (NIM/TTL) inputs that can be used for the **GATE**, the event discard in case of pile-up (**REJ**), and the GATE propagation (**GPO**). The Gate can be linear (same width as the external signal) or re-formed with programmable width.

The N6741 is provided with drivers for the supported communication interfaces, C libraries, demo software for an easy board understanding. Firmware upgrade can be performed via optical link or USB by the user.

Technical Specifications

GENERAL

- Form Factor: 1-unit wide, NIM module
- Weight: 870 g

ANALOG INPUT

Channels: 32 channels, Single-ended Offset: The Sliding Scale automatically manages the DAC for DC offset adjustment on each channel. Connector: 68-pin ERNI SMC with 1.27 mm pitch or 2 x 34 pin header-type male connector with 2.54 mm pitch Impedance: Zin = 2.5 kΩ Full Scale Range (FSR):

- 4 Vpp (3.75 Vpp with sliding scale enabled) or 8 Vpp (7.5 Vpp with sliding scale enabled)
- SW selectable

DIGITAL CONVERSION

- Resolution: 12 bits
- Sampling Rate: 62.5 MS/s simultaneously on each channel

CONVERSION GAIN

1k, 2k, 4k, 8k, 16k

DEAD TIME

50 ns

MINIMUM RISE TIME

2 ns

INTEGRAL NON LINEARITY (INL)

< 0.05 % in the range of (1:99) % of the FSR

DIFFERENTIAL NON LINEARITY (DNL)

< 1 %

ZERO SUPPRESSION

Zero Suppression threshold common to 8-channel groups and programmable in steps of ADC counts over the entire FSR

GATE

Gate mode with linear gate width or programmable by software.
The GATE signal is fed into the GATE LEMO connector.

Gate propagation: Gate_IN/Gate_OUT propagation through the GATE/GPO LEMO connectors

MEMORY

Multi-event Buffer of 1024 events

DIGITAL I/O

GATE (LEMO)

Front panel digital input of NIM/TTL logic: when high the event is acquired;

Z_{in} = 50 Ω

CLK-IN (AMP Modu II)

AC coupled differential input clock

LVDS, ECL, PECL, LVPECL, CML (single-ended NIM/TTL available by **A318** adapter)

Jitter <100ppm requested

GPO (LEMO)

Digital output that automatically propagates the GATE input

NIM/TTL; R_t = 50 Ω

REJ (LEMO)

Front panel digital input of NIM/TTL logic: when high the event is rejected

Z_{in} = 50 Ω

TIME STAMP

48-bit counter, 8 ns step, 16 ns resolution, 625 h range

ADC & MEM. CONTROLLER

Altera Cyclone EP1C16 (one FPGA serves 16 channels)

COMMUNICATION INTERFACE

USB

- USB 2.0 compliant
- Transfer rate up to 30 MB/s

Optical Link

- CAEN CONET proprietary protocol
- Up to 80 MB/s transfer rate
- Daisy chainable: it is possible to connect up to 8 or 32 ADC modules to a single Optical Link Controller (respectively **A2818** or **A3818**)

DPP FW SUPPORTED

Peak Sensing firmware

FIRMWARE UPGRADE

Firmware can be upgraded via USB/Optical Link

SOFTWARE

General purpose C libraries, configuration tools, readout software (Windows and Linux support)

POWER CONSUMPTIONS

3.6 A @ +6 V (typ.); 500 mA @ -6 V (typ.)

Ordering Options

Code	Description	
WN6741XAAAAA	N6741 32ch Peak Sensing ADC	RoHS

Accessories

A4818

USB 3.0 to CONET2 Adapter

A746D

Patch panel 32x LEMO 00 female to 1.27mm 68-pin ERNI SMC female

A318

Adapter for Clock signal FISCHER S101A004 male to 3-pin AMPMODU IV female – 10 cm

AI2700

Optical Fiber Series

A952

Cable assembly 2.54mm 34 pin female to 2.54mm 34 pin female - 50 cm

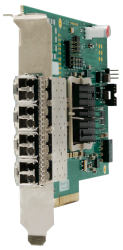
A385

Adapter 2.54mm 34-pin female to 16x LEMO 00 female (or MCX male) – 50 cm / 1 m

A317

Cable assembly for Clock distribution 3-pin AMPMODU IV female terminations – 18 cm / 25cm

A5818



CONET2 Controller based on PCI Express Gen 3 interface

Related Products

NIM8304

7U 12 slot smart fan unit Switching 2000 W Crate

NIM8303

5U 12 slot 300/600 W Crate

N957

8k Multi-Channel Analyzer

NIM8306

2 Slot Switching 750 W Mini Crate

NIM8305

2 Slot Switching 450 W Mini Crate

NIM8302P

5U 5 slot 150 W Portable Crate

V1741

64 Ch Peak Sensing ADC

N1068

16 ch Programmable Spectroscopy Amplifier and 16ch CFD

NV8020

7U CRATE VME/NIM 6 slot VME64 400W, 5 slot NIM 150W

Gallery

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