N6751

2/4 Channel 10 bit 2/1 GS/s Digitizer

Features

- 10 bit @ 2 GS/s (interleaved) or 1 GS/s
- Analog input on MCX coaxial connector (50 Ω, single-ended)
- 2-4 channels, NIM module
- 1 Vpp input dynamic range (0.2 Vpp **on request**) with programmable DC offset
- Algorithms for Digital Pulse Processing:
  - **Pulse Shape Discrimination (DPP-PSD)**
  - **Zero Length Encoding (DPP-ZLEplus)**
  -
- Time-stamped Waveform and List
- USB and Optical Link communication interfaces
- Multi-board synchronization features
- Daisy chain capability
- Compliant with **CoMPASS**, **DPP-ZLEplus Demo Software**, **CAENScope**, **CAEN WaveDump**, C and LabVIEW libraries

Description

The CAEN **Mod.N6751** is a digitizer able to **record waveforms** along with performing **advanced algorithms for online digital pulse processing (DPP)** of charge integration and pulse shape discrimination with constant fraction timing and zero-length encoding.

Data is read by a Flash ADC, **10-bit** resolution and **1 GS/s** sampling rate (**2 GS/s** using half of the channels in DES mode*), which is well suited for fast signals as the ones coming from fast organic, inorganic and liquid scintillators coupled to PMTs or Silicon Photomultipliers, Diamond detectors and others. The acquisition can be channel independent and it is possible to make coincidence/anti-coincidence logic among different channels and external veto/gating. Multiple boards can be synchronized to build up complex systems.

In the case of DPP mode, data can be saved in time-stamped list mode to support higher input rates and improve the throughput performances.
Piled-up events can be rejected or saved for offline analysis. The acquisition in DPP mode is fully controlled by the **CoMPASS** software, which manages the algorithm parameters, builds, plots and saves the relevant energy, time, and PSD spectra. In the case of waveform recording mode, the user can take advantage of the **CAENScope** and **WaveDump** software to access and save the waveforms.

Libraries and demo software in C and LabView are available for integration and customization of specific acquisition systems.

The N6751 comes in a **NIM** form factor with 2/4 input channels (2 channels in case of DES mode*). The communication to and from the board is provided through **USB** and **Optical Link** interfaces.

(*) *NOTE: DES mode is not available with DPP firmware*

Technical Specifications

GENERAL

16 general purpose LVDS I/O controlled by the FPGA: Run, Busy, Veto, Trigger and other functions can be programmed
An Input Pattern from the LVDS I/O can be associated to each trigger as an event marker

ANALOG INPUT

Firmware can be upgraded via VMEbus or Optical Link

DIGITAL CONVERSION

General purpose C libraries, configuration tools, readout software (Windows® and Linux® support), LabVIEW™ VIs and demos for Windows® only

SYSTEM PERFORMANCES

5.6 A @ +5V; 250 mA @ +12V, -12V not used

ADC CLOCK GENERATION

Form Factor
1-unit wide NIM

Weight
870 g

DIGITAL I/O

Channels
2/4 channels single-ended

Impedance
50 Ω

Bandwidth
500 MHz

Connector
MCX

Full-Scale Range
1 Vpp (default); 0.2 Vpp (on request)

Offset
Programmable DAC for DC
offset adjustment in the full range

Abs Max Rating
@1 Vpp: 3 Vpp (with Vrail max +3 V or –3 V for any DAC offset value)
@200 mVpp: 2 Vpp (with Vrail max +2 V or –2 V for any DAC offset value)

ACQUISITION MEMORY

Resolution
10 bits

Sampling Rate
1 GS/s (2 GS/s in DES mode)
Simultaneously on each channel
250 MS/s minimum by hardware down-sampling (see AN6308)

TRIGGER

- ENOB: 9.04 (56 kS Buffer)
- SINAD: 56.19 dB
- THD: 70.2 dB
- SFDR: 79.7 dB
- SIGMA: 0.58 LSB rms (56 kS buffer, open input)

SYNCHRONIZATION

- Clock source: internal/external
- Onboard programmable PLL provides generation of the main board clocks from an **internal** (50 MHz local Oscillator) or **external** (front panel CLK-IN connector) reference

ADC & MEMORY CONTROLLER FPGA

CLK-IN (AMP Modu II)
AC coupled differential input clock LVDS, ECL, PECL, LVPECL, CML (single ended NIM/TTL available by CAEN adapter)
Jitter < 100 ppm requested

GPO (LEMO)
General purpose digital output
NIM/TTL, Rt = 50 Ω

GPI (LEMO)
General purpose digital input
NIM/TTL, Zin = 50 Ω

TRG-IN (LEMO)
External trigger digital input
NIM/TTL, Zin = 50 Ω

COMMUNICATION INTERFACE

1.835 MS/ch (1.9 ms @ 1GS/s) or 3.6 MS/ch in DES mode (1.9 ms @ 2GS/s); 14.4 MS/ch (15 ms @ 1 GS/s) or 28.8 MS/ch in DES mode (15 ms @ 2 GS/s) divisible into 1 ÷ 1024 buffers
Independent read and write access
Programmable event size and pre/post-trigger

FIRMWARE

Trigger Source
Self-trigger: channel over/under threshold for either Common or Individual (DPP only) trigger generation
External-trigger: Common by TRG-IN connector
Software-trigger: Common by software command

Trigger Propagation
GPO digital output

Trigger Time Stamp
Waveform Recording: 31-bit counter, 16 ns resolution, 17 s range; 48-bit extension by firmware
DPP-PSD: 48-bit counter, 1 ns resolution, 78 h range; 10-bit and 1 ps fine time stamp with digital CFD
DPP-ZLEplus: 31-bit counter, 16 ns resolution, 17 s range; 48-bit extension by firmware

SOFTWARE

Clock Propagation
One-to-many: clock distribution from DT4700 to CLK-IN connector

Acquisition Synchronization
Sync Start/Stop through digital I/O (TRG-IN input, GPO output)

Trigger Time Stamp Alignment
By GPI input connector

POWER CONSUMPTIONS

Two Altera Cyclone EP3C16 (one FPGA serves 2 channels)

Accessories

AI2700

Optical Fiber Series

A317

Cable assembly for Clock distribution 3-pin AMPMODU IV female terminations – 18 cm / 25cm

A659

Cable assembly BNC male to MCX male – 1 m

A654

Cable assembly LEMO 00 male to MCX male – 1 m

A318

Adapter for Clock signal FISCHER S101A004 male to 3-pin AMPMODU IV female – 10 cm

Related Software

CAENSCOPE

Digitizer Software for Signal Inspection and Waveform Recording (New Version)

Related Firmware

DPP-SUP

Super Licence for CAEN Digitizers

D-WAVE

Digitizer Waveform Recording Firmware

DPP-ZLEPLUS

Digital Pulse Processing for the Zero Length Encoding

DPP-PSD

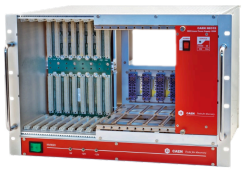
Digital Pulse Processing for Charge Integration and Pulse Shape Discrimination

Related Products

NIM8305

2 Slot Switching 450 W Mini Crate

NV8020A



7U CRATE VME/NIM 8 slot VME64 365W, 5 slot NIM 150W

NIM8306

2 Slot Switching 750 W Mini Crate

CAEN Upgrader

CAEN Upgrader

Firmware Upgrade Tool for Front-end Boards Bridges & VME Power Supply

NIM8304

7U 12 slot smart fan unit Switching 2000 W Crate

A4818

USB 3.0 to CONET2 Adapter

Gallery


Mod. N6751
DIGITIZER
LINK
CLK IN
CH0
TRG OUT
TRG IN
CH1
S IN
CH2
CH3
USB

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