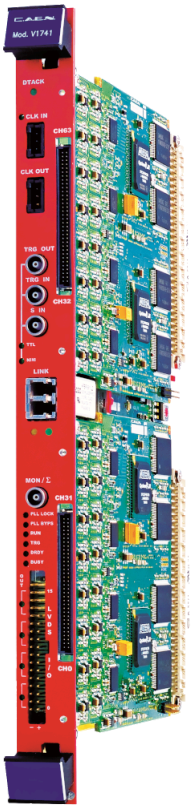
V1741

64 Ch Peak Sensing ADC

Features



- 1-unit wide 6U VME64 module
- 1k, 2k, 4k 8k, 16k Peak Sensing ADC
- 64 input channels, single-ended, with 68-pin Dual Row ERNI SMC connector (Zin: 2.5 kΩ)
  - Accepts positive and negative inputs
  - 4 Vpp or 8 Vpp Full Scale Range software selectable (3.75 Vpp and 7.5 Vpp when sliding scale is enabled)
- Common Gate mode (64 channels converted at once) with linear gate width or programmable by software
- Low dead time (about 50 ns after the previous gate closes)
- Sliding scale algorithm for DNL reduction
- Zero suppression with programmable threshold
- Multi-Event Buffer (1024 events)
- VME64 and Optical link (CAEN CONET proprietary protocol) communication interfaces
- Windows and Linux drivers, C libraries, demo software
- Firmware upgradable by the user

Description

The **V1741** is a **Digital Peak Sensing ADC** belonging to a new generation of detector readout systems based on a mixed analog-digital acquisition chain, combining a high channel density (**64 channels**) and a **low dead time**. The FLASH ADC architecture makes it possible to achieve an extremely low conversion time of the pulse peak, so new conversions take place less than 50 ns after the previous gates close.

Conversion gain ranges **from 1k up to 16k** channels with a low differential non-linearity (DNL) thanks to the *sliding scale method*.

Receiving the typical slow signal from a **Charge Sensitive Preamplifier** followed by a **Shaping Amplifier** (e.g. CAEN **N1068**), the FPGA identifies the peak of the pulse within a gate by means of digital filters. *The acquisition is common to all channels and takes place as soon as the GATE arrives.* The energy value together with the time of arrival of the event is first stored in a 1024 multi-event buffer and made available for the readout by VME bus or optical link interface (Daisy-chainable). *Both the energy spectrum and the list of events is available through the software interface.* Data throughput can be reduced by the Zero Suppression algorithm with a programmable threshold.

The front panel hosts LEMO (NIM/TTL) inputs that can be used for the **GATE**, the event discard in case of pile-up (**REJ**), and the GATE propagation (**GPO**). The Gate can be linear (same width as the external signal) or re-formed with programmable width.

The V1741 is provided with drivers for the supported communication interfaces, C libraries, demo software for an easy board understanding. Firmware upgrade can be performed via optical link or VMEbus by the user.

Technical Specifications

GENERAL

Form Factor: 1-unit wide, 6U VME64 module
Weight: 535 g

ANALOG INPUT

Channels: 64 channels, Single-ended Connector: 2 x 68-pin ERNI SMC with 1.27 mm pitch Impedance: Zin = 2.5 kΩ Offset: The Sliding Scale automatically manages the DAC for DC offset adjustment on each channel. Full Scale Range (FSR):

- 4 V_{pp} (3.75 V_{pp} with sliding scale enabled) or 8 V_{pp} (7.5 Vpp with sliding scale enabled)
- SW selectable

DIGITAL CONVERSION

Resolution: 12 bits
Sampling Rate: 62.5 MS/s simultaneously on each channel

CONVERSION GAIN

1k, 2k, 4k, 8k, 16k

DEAD TIME

50 ns

MINIMUM RISE TIME

2 ns

INTEGRAL NON LINEARITY (INL)

< 0.05 % in the range of (1:99) % of the FSR

DIFFERENTIAL NON LINEARITY (DNL)

< 1 %

ZERO SUPPRESSION

Zero Suppression threshold common to 8-channel groups and programmable in steps of ADC counts over the entire FSR

GATE

Gate mode with linear gate width or programmable by software. The GATE signal is fed into the GATE LEMO connector.

Gate propagation: Gate_IN/Gate_OUT propagation through the GATE/GPO LEMO connectors

MEMORY

Multi-event Buffer of 1024 events

DIGITAL I/O

CLK-IN (AMP Modu II)

- AC coupled differential input clock
- LVDS, ECL, PECL, LVPECL, CML
- (single ended NIM/TTL available by A318 adapter)
- Jitter<100ppm requested

GATE (LEMO)

- Front panel digital input of NIM/TTL logic: when high the event is acquired;
- Z_{in} = 50 Ω

CLK-OUT (AMP Modu II)

- DC coupled differential
- LVDS clock output locked at ADC sampling clock

GPO (LEMO)

- Digital output that automati cally propagates the GATE i nput
- NIM/TTL; R_t = 50 Ω

REJ (LEMO)

- front panel digital input of N IM/TTL logic: when high the event is rejected
- Z_{in} = 50 Ω

TIME STAMP

48-bit counter, 8 ns step, 16 ns resolution, 625 h range

LVDS I/O

16 general purpose LVDS I/O controlled by the FPGA: Run, Busy, Veto, Trigger and other functions can be programmed
An Input Pattern from the LVDS I/O can be associated to each trigger as an event marker

ADC & MEM. CONTROLLER

Altera Cyclone EP1C16 (one FPGA serves 16 channels)

COMMUNICATION INTERFACE

Optical Link

- CAEN CONET proprietary protocol
- Up to 80 MB/s transfer rate
- Daisy chainable: it is possible to connect up to 8 or 32 ADC modules to a single O ptical Link Controller (respectively **A2818** or **A3818**)

VME

- VME 64X compliant
- Data transfer mode: BLT32, MBLT64
- (70 MB/s using CAEN Bridge),
- CBLT32/64, 2eVME, 2eSST (up to 200 MB/s)

DPP FW SUPPORTED

Peak Sensing firmware

FIRMWARE UPGRADE

Firmware can be upgraded via VMEbus/Optical Link

SOFTWARE

General purpose C libraries, configuration tools, readout software (Windows and Linux support)

POWER CONSUMPTIONS

5.4 A @ +5 V; 270 mA @ +12 V, -12 V not used

Ordering Options

Code	Description	
WV1741XAAAAA	V1741 64ch Peak Sensing ADC	RoHS

Accessories

A4818

USB 3.0 to CONET2 Adapter

A318

Adapter for Clock signal FISCHER S101A004 male to 3-pin AMPMODU IV female – 10 cm

AI2700

Optical Fiber Series

A746B

Patch panel 64x LEMO 00 female to two x 1.27mm 68-pin ERNI SMC female

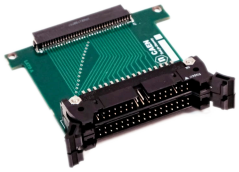
A385

Adapter 2.54mm 34-pin female to 16x LEMO 00 female (or MCX male) – 50 cm / 1 m

A317

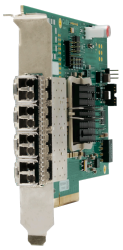
Cable assembly for Clock distribution 3-pin AMPMODU IV female terminations – 18 cm / 25cm

A371



Adapter 2.54mm 34x2 pin male to 1.27mm 68-pin ERNI SMC female

A5818



CONET2 Controller based on PCI Express Gen 3 interface

Related Products

VME8004X

2U 4 Slot VME64X Mini Crate

VME8011

7U 21 Slot VME64 Low Cost Crate

VME8100

8U 21 Slot VME64/64X Enhanced Crate Series

VME8010

7U 21 Slot VME64 Low Cost Crate

VX4718

VME to USB 3.0/Ethernet/Optical Link Bridge

VME8004B

2U 4 Slot VME64 Mini Crate

VME8008X

4U 8 Slot VME64X Mini Crate

VME8200

9U 21Slot VME64X Enhanced Crate series

µ-crate

Desktop single-slot VME64X Crate

VME8008XB

A4818

USB 3.0 to CONET2 Adapter

VME8008B

4U 8 Slot VME64 Mini Crate

V3718

VME to USB 2.0 / Optical Link Bridge

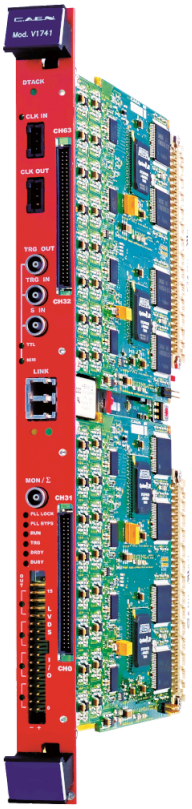
VX3718

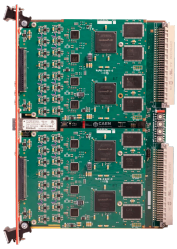
VME64 to USB 2.0/Optical Link Bridge

V4718

VME to USB 3.0/Ethernet/Optical Link Bridge

Gallery


Mod. V1741
DTACK
CLK IN
CH63
CLK OUT
TRG OUT
TRG IN
S IN
CH32
TTL
NIM
LINK
MON / Σ
CH31
PLL LOCK
PLL STATUS
RUN
TRG
BUSY
CH0



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