VX1743

16 Input Channel 12bit 3.2 GS/s Switched Capacitor Digitizer

Features

- 12-bit @ 3.2 GS/s ADC
- Switched Capacitor technology based on the SAMLONG chip (CEA/IRFU & CNRS/IN2P3/LAL Orsay)
  - 1024 capacitor cells per channel (acquisition window of ~ 320 ns @ 3.2 GS/s)
- 3.2 GS/s , 1.6 GS/s, 800 MS/s, 400 MS/s software selectable sampling frequencies
- 16 input channels, single-ended
- Max. AD conversion dead-time: 125 µs @1024 samples
- 2.5 Vpp input range
- 16-bit programmable DC offset adjustment in the full range independently on each channel
- Trigger Time stamps
- Memory buffer (max.): 7 events/ch @1024 S/event
- Pre-post trigger adjustment
- Max. AD conversion dead-time: 125 µs @1024 samples
- Real time hit counting independent of acquisition rate on each channel
- On-board charge calculation for fast histogramming (user-defined integration window)
- One embedded pulser per channel for test and reflectometry applications
- Front panel clock input/output available for multiboard synchronization (direct feed through or PLL-based synthesis)
- 16 programmable LVDS I/Os
- Optical Link interface (CONET proprietary protocol) Daisy-chainable through **A5818** (PCIe Gen 3) Controller or **A4818** (USB3-to-CONET)
- VME64X interface
- Firmware upgradeable via VME*bus*/Optical Link
- Fully controlled by the **WaveCatcher** readout software

Description

The CAEN **Mod. VX1743** is a Waveform Digitizer, in VME64X form factor, housing **16** Channel **12** bit **3.2 GS/s** ADC stage based on Switched Capacitor Digitizer arrays. This technology makes it suited for typical applications like precise characterization of high speed detectors (PMTs, SiPMs, APDs,...) and High Resolution Photon timing with MCP-PMTs.

The Switched Capacitor Array is **SAMLONG chip** (designed by LAL Orsay & CEA/IRFU in collaboration with CNRS/IN2P3), implementing a series of **1024** capacitors (analog memory) in which the analog input signal is **continuously sampled** in a circular way. The default sampling frequency is 3.2 GHz, while 1.6 GHz, 800 MHz, and 400 MHz can be software selected.

The input signal is continuously sampled at high frequency in the SAMLONG array of capacitive cells (holding phase) until the trigger arrival. The trigger stops the sampling, the analog memory buffer is frozen, and the cell content is sent to the 12-bit ADC to be digitized at lower frequency. The non-simultaneity between the Sample & Hold phase and the digital conversion generates a dead-time (up to 125 µs @1024 samples).

The acquisition takes place upon different global trigger sources, which can be the external TRG-IN, software , or the logic combination of local channel under-/over-thresholds generated from individual discriminator with programmable threshold.

The VX1743 features an embedded **Charge Mode**, where the pulse integration window is defined by the user (high rates ~3.5 kEvents/s). This feature allows to perform on-line processing on detector signal directly digitized.

The events are stored into the channel digital memory (up to 7 events/ch @1024 samples) to be read out through the **VMEBus** or **Optical Link** interfaces. Multiple boards can be synchronized to build up complex systems.

This Digitizer is fully supported by **WaveCatcher** software, while libraries and demo software in C, Phyton, and LabView are available for integration and customization of specific acquisition systems.

Note: VX1743 can be operated with **VME8004X** / **VME8008X** / **VME8100** / **VME8200**/**µ-crate**.

Technical Specifications

GENERAL

- Weight: 535 g
- Form Factor: 1-unit wide VME64X
- Dimension: 6U x 160 mm

ANALOG INPUT

- Number of Inputs: 16, single-ended, DC coupled
- Bandwidth (-3dB): 500 MHz
- Impedance: 50 Ω
- Connector Type: MCX
- Full Scale Range: 2.5 Vpp
- 16-bit programmable DC offset adjustment in the full range independently on each channel
- Abs. Max. Voltage Rating: 3.5 Vpp (with Vrail max +3.5V or -3.5V) for any DAC offset in single ended configuration

DIGITAL CONVERSION

- Resolution: 12 bits
- Sampling Rate:
  - 3.2 GS/s default
  - 1.6 GS/s, 0.8 GS/s, 0.4 GS/s software selectable
- Switched Capacitor Array: SAMLONG chip, 8 channels with 1024 storage cells each
- Dead-time: max. 125 µs @1204 samples (decreasing with programmable lower record lengths)

TEST FUNCTION

- One pulse generator per channel
- 16-bit programmable pulse pattern
- Fixed amplitude: ~0.7 V with floating input
- Pattern period: 3.5 µs

SYSTEM PERFORMANCES

Sampling Time Precision

- < 20 ps @ 3.2 GS/s (before calibration)
- < 5 ps @ 3.2 GS/s (after calibration)

Note: obtained with factory calibration and dual-pulse timing measurement with pulse generator.

Test conditions

- Periodic input pulses with 1-V Amplitude
- 1-kHz Frequency Rise time of 0.8 / 1.6 / 2.5 ns.

The resolution does not change significantly when varying the delay Δt between the two pulses.

Noise Level

0.75 mV RMS

DIGITIAL I/O

LVDS I/O

- 16 differential pairs
- I/O functions: Sync, Data Ready, Memory full, Trigger Out, Clear, etc.
- LVDS
- Zdiff = 100 Ω (when set as inputs)
- 2.54mm 34-pin AMPMODU Mod II male connector

TRG-IN/TRG-OUT/S-IN

- General-purpose digital I/Os
- Sigle-ended TTL/NIM
- LEMO 00 male connector
- Software programmable function (trigger, sync, busy, start, etc.)
- TRG-IN/S-IN: internally terminated with 50 Ω (Zin = 50 Ω)
- TRG-OUT requires Rt = 50 Ω

ANALOG OUT

- Software programmable DAC output (12-bit/100MHz) with two operating modes:
  - Majority signal: proportional to the number of channels (enabled) under/over threshold (1 step = 125 mV)
  - Buffer Occupancy: DC voltage level increasing in fixed steps of 0.976 mV with the memory filling with events (step value can be increased)

ACQUISITION MEMORY

- 7 full event/ch Multi-event buffer (1024 S/event, that is 320 ns/event @ 3.2 GS/s)
- Independent read and write access
- Programmable event size and pre/post-trigger

COMMUNICATION INTERFACE

VMEbus

- VME64X
- Data modes: D32, BLT32, MBLT64, CBLT32/64, 2eVME, 2eSST, Multi Cast Cycles
- Transfer Rate: 60 MB/s (MBLT64), 100 MB/s (2eVME), 160 MB/s (2eSST)
- Sequential and random access to the data of the Multi Event Buffer
- The Chained readout allows to read one event from all the boards in a VME crate with a BLT access

Optical Link

- CAEN proprietary CONET protocol
- Transfer Rate: up to 80 MB/s
- Daisy Capability: up to 8 ADC modules per single optical link by A5818 Controller or A4818 Adapter

TRIGGER AND EVENT ACQUISITION

Triggered Mode

All the channels fire simultaneously upon a global trigger generated by the Central Logic Unit receiving the trigger source signals.

Trigger Sources

- Software by register writing
- External upon the leading edge of The TRG-IN signal (TTL/NIM)
- Local (self-trigger) upon the channel discriminator with programmable threshold

Trigger Timestamp – Waveform Rec. firmware

- Resolution: 5 ns
- Counter range:40 bits
- Full-scale range: ~ 83 min

SYNCHRONIZATION

Clock Generation

By default, the Digitizer's main clocks are generated upon a 50MHz reference frequency that can optionally be internal (50MHz local Oscillator) or external (CLK-IN). Onboard programmable PLL allows locking to different external frequencies.

Clock Synchronization

Default 50MHz frequency distributed by:

- Fan-in into CLK-IN (**DT4700**)
- CLK-IN/CLK-OUT Daisy chain with sw programmable CLK-OUT delay shift

Run Synchronization (Acquisition Start/Stop)

Optionally, by Daisy chain or fan-in propagation through differential LVDS I/Os, or single-ended NIM/TTL I/O.

CLK-IN/CLK-OUT Connector

- Reference clock differential signal
- 2.54mm 3-pin AMPMODU Mod II male connector
- CLK-IN: AC-coupled LVDS, ECL, PECL, LVPECL, CML (Zdiff = 100 Ω)
- CLK-OUT: LVDS

Data Synchronization

Programmable Busy/Veto logic on differential LVDS I/O or single-ended NIM/TTL I/O for event building.

Trigger Distribution

TRG-IN/TRG-OUT NIM/TTL LEMO I/O (global trigger) or LVDS I/O (global or local trigger).

FPGA

- Altera Cyclone EP3C16
- 1 FPGA serves 4 channels

CAEN FIRMWARE

Waveform Recording Firmware (Freeware)

- Default mode: waveform recording
- Charge mode: charge integration, software selectable

Upgrades (Free)

Web available CFA files for Waveform Recording firmware upgrade through the CAEN Toolbox software, via VMEbus or Optical Link.

SOFTWARE

Readout Software for Waveform Rec. Firmware (Freeware)

CAEN WaveCatcher: GUI-based application for the 743 Digitizer series, developed in LabWindows/CVI by CNRS/IN2P3/LAL, and capable to fully control single-board and multi-board syncronized systems.

SDK and Tools (Freeware)

General-purpose libraries (C/Python, LabVIEW) with demo samples for host Windows® and Linux® PC.

ENVIRONMENTAL

- **Environment:** Indoor use
- **Operating Temperature**: 0°C to +40°C
- **Storage Temperature**: -10°C to +60 °C
- **Operating Humidity:** 10% to 90% RH non condensing
- **Storage Humidity:** 5% to 90% RH non condensing
- **Pollution Degree:** 2
- **Overvoltage Category:** II
- **EMC Environment:** Commercial and light industrial
- **IP Degree:** Enclosure (desktop models), not for wet location

REGULATORY COMPLIANCE

- EMC: CE 2014/30/EU Electromagnetic Compatibility Directive
- Safety: CE 2014/35/EU Low Voltage Directive

POWER CONSUMPTIONS

+5 V: 4 A (Typ.)
+12 V: 0.625 A (Typ.)
-12 V: not used

Ordering Options

Code	Description	
WVX1743XAAAA	VX1743 - 16 Ch. 12 bit 3.2GS/s Switched-Capacitor Digitizer: 7 events/ch (1kS/event), EP3C16, SE	RoHS

Accessories

A316

Cable assembly 2.54mm 2-pin header female - 5 cm

AI2700

Optical Fiber Series

A952

Cable assembly 2.54mm 34 pin female to 2.54mm 34 pin female - 50 cm

A318

Adapter for Clock signal FISCHER S101A004 male to 3-pin AMPMODU IV female – 10 cm

A319B

Clock cable assembly from Digitizer Series 1.0 to Digitizer Series 2.0 - 20cm

DT4700

Clock Generator and FAN-OUT

A654

Cable assembly LEMO 00 male to MCX male – 1 m

A954

Cable assembly 2.54mm 34 pin female to two 2.54mm 16 pin female - 50 cm

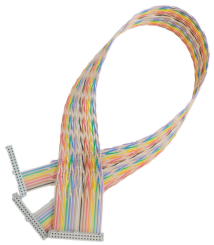
A317

Cable assembly for Clock distribution 3-pin AMPMODU IV female terminations – 18 cm / 25cm

A659

Cable assembly BNC male to MCX male – 1 m

A953



Cable assembly 2.54mm 34 pin female to two 2.54mm 34 pin female – 50 cm

Related Software

CAEN Toolbox

Multi-Functional Software Suite for the Upgrade of Front-end Boards, Bridges and Power Supplies

Related Firmware

D-WAVE

Digitizer Waveform Recording Firmware

Related Software Libraries

CAENDigitizer Library

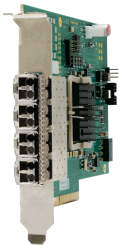
Library of functions for CAEN Digitizers high level management

CAENComm Library

Interface library for CAEN Data Acquistion Modules

Related Products

A5818



CONET2 Controller based on PCI Express Gen 3 interface

VME8004X

2U 4 Slot VME64X Mini Crate

VME8100

8U 21 Slot VME64/64X Enhanced Crate Series

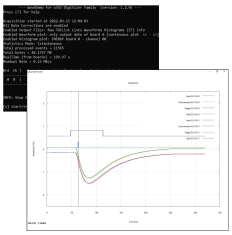
VME8200

9U 21Slot VME64X Enhanced Crate series

µ-crate

Desktop single-slot VME64X Crate

WaveDemo x743



CAEN x743 Digitizer Readout Application

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VME8008X

4U 8 Slot VME64X Mini Crate

VX4718

VME to USB 3.0/Ethernet/Optical Link Bridge

A4818

USB 3.0 to CONET2 Adapter

DT5743

8 Input Channel 12bit 3.2 GS/s Switched Capacitor Digitizer

WAVECATCHER

Oscilloscope Tool for 743 digitizer family

VX3718

VME64 to USB 2.0/Optical Link Bridge

Gallery

CAEN S.p.A.
Via Vetraia 11
55049 - Viareggio
Italy
Phone +39.0584.388.398
Fax +39.0584.388.959
info@caen.it
www.caen.it

CAEN GmbH
Brunnenweg 9
64331 Weiterstadt, Germany
Phone +49 (0)212.254.4077
Mobile +49 (0)151.16.548.484
info@caen-de.com
www.caen-de.com

CAEN Technologies, Inc.
1 Edgewater Street - Suite 101
Staten Island, NY 10305
USA
Phone +1.718.981.0401
Fax +1.718.556.9185
info@caentechnologies.com
www.caentechnologies.com

CAENspa India Private Limited
B205, BLDG42, B Wing,
Azad Nagar Sangam CHS,
Mhada Layout, Azad Nagar, Andheri West
Mumbai, Maharashtra 400053, India
info@caen-india.in
www.caen-india.in