VX1751

4/8 Input Channel 10 bit 2/1 GS/s Digitizer

Features

- 10 bit 1 GS/s (2 GS/s in DES mode) ADC
- FPGA for real-time data processing:
  - **Pulse Shape Discrimination (DPP-PSD)**
  - **Zero Length Encoding (DPP-ZLEplus)**
- 8 input channels (4 in DES mode), single-ended
- 1 Vpp input range (default); 0.2 Vpp customization **by ordering option**
- 16-bit programmable DC offset adjustment in the full range independently on each channel
- Trigger Time stamps
- Multi-Event Memory buffer: 1.835 MS/ch (3.6 MS/ch in DES mode) or 14.4 MS/ch (28.8 MS/ch in DES mode) divisible into 1 ÷ 1024 buffers
- Programmable event size and pre-post trigger adjustment
- Analog Sum/Majority and digital over/under threshold flags for Global Trigger logic
- Front panel clock input/output available for multiboard synchronization (direct feed through or PLL-based synthesis)
- 16 programmable LVDS I/Os
- Optical Link interface (CONET proprietary protocol) Daisy-chainable through **A5818** (PCIe Gen 3) Controller or **A4818** (USB3-to-CONET)
- VME64X interface
- Firmware upgradeable via VME/Optical Link
- Fully supported by **CoMPASS** and **WaveDump2** software

Description

The **CAEN Mod. VX1751** is a Waveform Digitizer, in VME64X form factor, housing **8** Input Channel **10** bit **1 GS/s** Flash ADC, designed for waveform recording and supporting advanced algorithms for online digital pulse processing (DPP) making charge integration and pulse shape discrimination (PSD), and data reduction by zero-length encoding (ZLEplus). If the DES mode* (Dual Edge Sampling) is enabled, this device becomes a 4 input channel 10 bit 2 GS/s Waveform Digitizer.

The Digitizer is well suited for fast signals as the ones coming from fast organic, inorganic and liquid scintillators coupled to PMTs or Silicon Photomultipliers, Diamond detectors and others. The acquisition can be channel independent and it is possible to make coincidence/anti-coincidence logic among different channels and external veto/gating. Multiple boards can be synchronized to build up complex systems.

In the case of DPP mode, users can acquire quantitative physical parameters (Time, Integrated Charge, Pulse Shape Discrimination with very fine time resolution) as well as read out waveforms with baseline suppression on channel basis (Zero-Length Encoding) The acquisition in **DPP-PSD** mode is fully controlled by the **CoMPASS** software, which manages the algorithm parameters, builds, plots and saves the relevant energy, time, and PSD spectra. In the case of waveform recording mode, the user can take advantage of the **WaveDump** and **WaveDump2** software to access and save the waveforms. A C-based demo is provided to configure the algorithm parameters, control the data acquisition, saving, and plotting for the **DPP-ZLEPlus** mode.

Libraries and demo software in C, Phyton, and LabView are available for integration and customization of specific acquisition systems.
The communication to and from the board is provided through the **VMEBus** and **Optical Link** interfaces.

(*) *NOTE: DES mode is not available with DPP firmware*

Note: VX1751 can be operated with **VME8004X**/ **VME8008X** /**VME8100** / **VME8200**/**µ-crate**.

Technical Specifications

GENERAL

- Weight: 535 g
- Form Factor: 1-unit wide VME64X
- Dimension: 6U x 160 mm

ANALOG INPUT

- Number of Inputs: 8/4, single-ended, DC coupled
- Bandwidth (-3dB): 500 MHz
- Impedance: 50 Ω
- Gain: x1, fixed
- Connector Type: MCX
- Full Scale Range: 1 Vpp default; 0.2 Vpp customization by ordering option
- 16-bit programmable DC offset adjustment in the full range independently on each channel
- Abs. Max. Voltage Rating:
  - 3 Vpp @1 Vpp (with Vrail max +3 V or –3 V for any DAC offset value)
  - 2 Vpp @0.2 Vpp (with Vrail max +2 V or –2 V for any DAC offset value)

DIGITAL CONVERSION

- Resolution: 10 bits
- Sampling Rate:
  - 1 GS/s simultaneously on each channel (default)
  - 2 GS/s in DES mode (half channels supported)
  - Down to 250 MS/s by hardware downsampling (**AN6308**)

SYSTEM PERFORMANCES

- ENOB: 9.04 (56 kS Buffer)
- SINAD: 56.19 dB
- THD: 70.2 dB
- SFDR: 79.7 dB
- SIGMA: 0.58 LSB rms (56 kS buffer, open input)

DIGITAL I/O

LVDS I/O

- 16 differential pairs
- Sw programmable I/O function (individual self-trigger outputs, trigger validations, Veto, Busy, Start, Stop, Pattern Input, etc.)
- LVDS
- Zdiff = 100 Ω (when set as inputs)
- 2.54mm 34-pin AMPMODU Mod II male connector

TRG-IN/TRG-OUT/S-IN

- General-purpose digital I/Os
- Sigle-ended TTL/NIM
- LEMO 00 male connector
- Software programmable function (trigger, veto, busy, etc.)
- TRG-IN/S-IN: internally terminated with 50 Ω (Zin = 50 Ω)
- TRG-OUT requires Rt = 50 Ω

ANALOG OUT

- Software programmable DAC output (12-bit/125MHz) with four operating modes:
  - Test Waveform: 1 Vpp test ramp generator
  - Majority signal: proportional to the number of channels (enabled) under/over threshold (1 step = 125 mV)
  - Buffer Occupancy: output signal is proportional to the Multi Event Buffer Occupancy (1 buffer ~ 1 mV)
  - Voltage level: output signal is a programmable voltage level (0 to +1 V range with 12-bit resolution)

ACQUISITION MEMORY

- 1.835 MS/ch (1.9 ms @ 1GS/s), that is 3.6 MS/ch in DES mode (1.9 ms @ 2GS/s) or 14.4 MS/ch (15 ms @ 1 GS/s) that is 28.8 MS/ch in DES mode (15 ms @ 2 GS/s) Multi-event Buffer divisible into 1 ÷ 1024 buffers
- Independent read and write access
- Programmable event size and pre/post-trigger

COMMUNICATION INTERFACE

VMEbus

- VME64X
- Data modes: D32, BLT32, MBLT64, CBLT32/64, 2eVME, 2eSST, Multi Cast Cycles
- Transfer Rate: 60 MB/s (MBLT64), 100 MB/s (2eVME), 160 MB/s (2eSST)
- Sequential and random access to the data of the Multi Event Buffer
- The Chained readout allows to read one event from all the boards in a VME crate with a BLT access

Optical Link

- CAEN proprietary CONET protocol
- Transfer Rate: up to 80 MB/s
- Daisy Capability: up to 8 ADC modules per single optical link by A5818 Controller or A4818 Adapter

TRIGGER AND EVENT ACQUISITION

Triggered Mode

All the channels fire simultaneously upon a global trigger generated by the Central Logic Unit receiving the trigger source signals; a zero suppression function is available.

Streaming Readout Mode

Each channel autonomously identifies the ROI and uses the local trigger to get events independently on the other channels; validation logics can be configured for correlated acquisition (coincidence/anticoincidence).

Trigger Sources

- Software by register writing
- External upon the leading edge of The TRG-IN signal (TTL/NIM)
- Local (self-trigger) upon the channel discriminator with programmable threshold

Trigger Timestamp – Waveform Rec. firmware

- Resolution: 16 ns
- Counter range: 31 bits (default); extendable to 48-bit by firmware
- Full-scale range: ~ 17 s @31-bit

Trigger Timestamp – DPP firmware

DPP-PSD:

- Resolution: 1 ns
- Counter Range: 48 bits
- Full-scale range: ~ 78 h
- Digital CFD: 10-bit, 1 ps fine timestamp

DPP-ZLEplus:

- Resolution: 16 ns
- Counter Range: 31-bit (default); extendable to 48-bit by firmware
- Full-scale range: ~ 17 s @31-bit

SYNCHRONIZATION

Clock Generation

By default, the Digitizer's main clocks are generated upon a 50MHz reference frequency that can optionally be internal (50MHz local Oscillator) or external (CLK-IN). Onboard programmable PLL allows locking to different external frequencies.

Clock Synchronization

Default 50MHz frequency distributed by:

- Fan-in into CLK-IN (**DT4700**)
- CLK-IN/CLK-OUT Daisy chain with sw programmable CLK-OUT delay shift

PLL programming files for supported custom frequencies can be generated and loaded by the CAEN Toolbox software.

Run Synchronization (Acquisition Start/Stop)

Optionally, by Daisy chain or fan-in propagation through differential LVDS I/O, or single-ended NIM/TTL I/O.

CLK-IN/CLK-OUT Connector

- Reference clock differential signal
- 2.54mm 3-pin AMPMODU Mod II male connector
- CLK-IN: AC-coupled LVDS, ECL, PECL, LVPECL, CML (Zdiff = 100 Ω)
- CLK-OUT: LVDS

Data Synchronization

Programmable Busy/Veto logic on differential LVDS I/O, or single-ended NIM/TTL I/O for event building.

Trigger Distribution

TRG-IN/TRG-OUT NIM/TTL LEMO I/O (global trigger) or LVDS I/O (global or local trigger).

FPGA

- Altera Cyclone EP3C16
- One FPGA serves 2 channels

CAEN FIRMWARE

DPP Firmware (Shareware)

Pay firmware implementing a digital pulse processing algorithm:

- **DPP-PSD**: Charge Integration and Pulse Shape Discrimination
- **DPP-ZLEplus**: Zero Length Encoding

30-minute per power cycle in Trial mode; license is required for full-time work.

Waveform Recording Firmware (Freeware)

Designed for waveform recording.

Upgrades (Free)

Web available CFA files for Waveform Recording and DPP firmware upgrade through the CAEN Toolbox software, via VMEbus or Optical Link.

SOFTWARE

Readout Software for Waveform Rec. Firmware (Freeware)

- **CAEN WaveDump**: Digitizer 1.0 series support, single-board management, user-customizable
- **WaveDump2**: Digitizer 1.0 and 2.0 series support, single and multi-board management, GUI based

Readout Software for DPP Firmware (Freeware)

- **CoMPASS**: Digitizer 1.0 and 2.0 series support, single and multi-board management, GUI based
- **DPP-ZLEplus Readout Demo**: sample code with C source files to dial with the ZLE functionalities and help in user's DAQ development

SDK and Tools (Freeware)

General-purpose libraries (C/Python, LabVIEW) with demo samples for host Windows® and Linux® PC.

ENVIRONMENTAL

- **Environment:** Indoor use
- **Operating Temperature**: 0°C to +40°C
- **Storage Temperature**: -10°C to +60 °C
- **Operating Humidity:** 10% to 90% RH non condensing
- **Storage Humidity:** 5% to 90% RH non condensing
- **Pollution Degree:** 2
- **Overvoltage Category:** II
- **EMC Environment:** Commercial and light industrial
- **IP Degree:** Enclosure (desktop models), not for wet location

REGULATORY COMPLIANCE

- EMC: CE 2014/30/EU Electromagnetic Compatibility Directive
- Safety: CE 2014/35/EU Low Voltage Directive

POWER CONSUMPTIONS

+5V: 6.5 A (Typ.)

+12V: 0.2 A (Typ.)

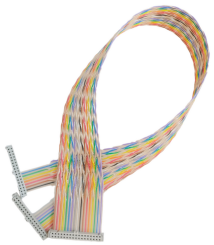
-12V: 0.3 A (Typ.)

Ordering Options

Code	Description	
WVX1751CXAAA	VX1751C - 4/8 Ch. 10 bit 2/1 GS/s Digitizer: 28.8/14.4MS/ch, EP3C16, SE	RoHS
WVX1751XAAAA	VX1751 - 4/8 Ch. 10 bit 2/1 GS/s Digitizer: 3.6/1.8MS/ch, EP3C16, SE	RoHS

Accessories

A953



Cable assembly 2.54mm 34 pin female to two 2.54mm 34 pin female – 50 cm

A316

Cable assembly 2.54mm 2-pin header female - 5 cm

A317

Cable assembly for Clock distribution 3-pin AMPMODU IV female terminations – 18 cm / 25cm

A952

Cable assembly 2.54mm 34 pin female to 2.54mm 34 pin female - 50 cm

A654

Cable assembly LEMO 00 male to MCX male – 1 m

A954

Cable assembly 2.54mm 34 pin female to two 2.54mm 16 pin female - 50 cm

A659

Cable assembly BNC male to MCX male – 1 m

DT4700

Clock Generator and FAN-OUT

A319B

Clock cable assembly from Digitizer Series 1.0 to Digitizer Series 2.0 - 20cm

A318

Adapter for Clock signal FISCHER S101A004 male to 3-pin AMPMODU IV female – 10 cm

AI2700

Optical Fiber Series

Related Software

CAEN SyncTest

Software Demo for CAEN Digitizers Synchronization

CAEN Toolbox

Multi-Functional Software Suite for the Upgrade of Front-end Boards, Bridges and Power Supplies

COMPASS

Multiparametric DAQ Software for Physics Applications

WAVEDUMP2

Open Source Software for Digitizer 2.0 and 1.0 Series

WaveDump

Readout Application for CAEN Digitizer 1.0

Related Firmware

D-WAVE

Digitizer Waveform Recording Firmware

DPP-ZLEPLUS

Digital Pulse Processing for the Zero Length Encoding

DPP-SUP

Super Licence for CAEN Digitizers

DPP-PSD

Digital Pulse Processing for Charge Integration and Pulse Shape Discrimination

Related Software Libraries

CAENComm Library

Interface library for CAEN Data Acquistion Modules

CAEN FELib Library

High level library for CAEN Digitizers 2.0

CAENDigitizer Library

Library of functions for CAEN Digitizers high level management

Related Products

VME8200

9U 21Slot VME64X Enhanced Crate series

DT5751

2/4 Input Channel 10 bit 2/1 GS/s Digitizer

VME8008X

4U 8 Slot VME64X Mini Crate

µ-crate

Desktop single-slot VME64X Crate

VX4718

VME to USB 3.0/Ethernet/Optical Link Bridge

V1751

4/8 Input Channel 10 bit 2/1 GS/s Digitizer

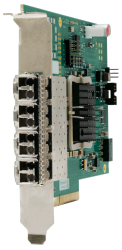
VME8004X

2U 4 Slot VME64X Mini Crate

VME8100

8U 21 Slot VME64/64X Enhanced Crate Series

A5818



CONET2 Controller based on PCI Express Gen 3 interface

VX3718

VME64 to USB 2.0/Optical Link Bridge

A4818

USB 3.0 to CONET2 Adapter

Gallery

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