VX1761

2 Input Channel 10 bit 4GS/s Digitizer

Features

- 10 bit 4 GS/s ADC
- 2 inputs channels, single-ended)
- 1 Vpp input range
- 16-bit programmable DC offset adjustment in the full range independently on each channel
- Trigger Time stamps
- Multi-Event Memory buffer: 7.2 MS/ch or 57.6 MS/ch divisible into 1 ÷ 1024 buffers
- Programmable event size and pre-post trigger adjustment
- Analog Sum/Majority and digital over/under threshold flags for Global Trigger logic
- Front panel clock input/output available for multiboard synchronization (direct feed through or PLL-based synthesis)
- 16 programmable LVDS I/Os
- Optical Link interface (CONET proprietary protocol) Daisy-chainable through **A5818** (PCIe Gen 3) Controller or **A4818** (USB3-to-CONET)
- VME64X interface
- Firmware upgradeable via VME/Optical Link
- Fully supported by **WaveDump** software

Description

The **CAEN Mod. VX1761** is a Waveform Digitizer, in VME64X form factor, with the **highest sampling rate** Flash ADC (**10 bit @ 4GS/s**), designed for waveform recording.

The Digitizer is well suited for **fast signals** from fast organic, inorganic and liquid scintillators coupled to PMTs or Silicon Photomultipliers, Diamond detectors and others. The data stream is written in a circular memory buffer with independent read/write access, which reduces the dead-time of the acquisition process. Basing on the waveform recording mode, the events are saved simultaneously on all the channels upon the trigger arrival. Majority and gate functions can be applied. Multiple boards can be synchronized to build up complex systems.

The acquisition is fully controlled by **CAEN WaveDump** software, which manages the settings, plots and saves the waveforms. Libraries and demo software in C, Phyton, and LabView are available for integration and customization of specific acquisition systems.

The communication to and from the board is provided through **VMEBus** and **Optical Link** interfaces.

Note: VX1761 can be operated with **VME8004X** / **VME8008X** / **VME8100** / **VME8200**/**µ-crate**.

Technical Specifications

GENERAL

- Weight: 600 g
- Form Factor: 1-unit wide VME64X
- Dimension: 6U x 160 mm

ANALOG INPUT

- Number of Inputs: 2, single-ended, DC coupled
- Bandwidth (-3dB): 1 GHz
- Impedance: 50 Ω
- Gain: x1, fixed
- Connector Type: MCX
- Full Scale Range: 1 Vpp
- 16-bit programmable DC offset adjustment in the full range independently on each channel
- Abs. Max. Voltage Rating: 3 Vpp (with Vrail max +3 V or –3 V for any DAC offset value)

DIGITAL CONVERSION

- Resolution: 10 bits
- Sampling Rate: 4 GS/s Simultaneously on each channel

DIGITAL I/O

LVDS I/O

- 16 differential pairs
- Sw programmable I/O function (individual self-trigger outputs, trigger validations, Veto, Busy, Start, Stop, Pattern Input, etc.)
- LVDS
- Zdiff = 100 Ω (when set as inputs)
- 2.54mm 34-pin AMPMODU Mod II male connector

TRG-IN/TRG-OUT/S-IN

- General-purpose digital I/Os
- Sigle-ended TTL/NIM
- LEMO 00 male connector
- Software programmable function (trigger, veto, busy, etc.)
- TRG-IN/S-IN: internally terminated with 50 Ω (Zin = 50 Ω)
- TRG-OUT requires Rt = 50 Ω

ANALOG OUT

- Software programmable DAC output (12-bit/125MHz) with four operating modes:
  - Test Waveform: 1 Vpp test ramp generator
  - Majority signal: proportional to the number of channels (enabled) under/over threshold (1 step = 125 mV)
  - Buffer Occupancy: output signal is proportional to the Multi Event Buffer Occupancy (1 buffer ~ 1 mV)
  - Voltage level: output signal is a programmable voltage level (0 to +1 V range with 12-bit resolution)

ACQUISITION MEMORY

- 7.2 MS/ch (1.9 ms @ 4 GS/s) or 57.6 MS/ch (15 ms @ 4 GS/s) Multi-event Buffer divisible into 1 ÷ 1024 buffers
- Independent read and write access
- Programmable event size and pre/post-trigger

COMMUNICATION INTERFACE

VMEbus

- VME64X
- Data modes: D32, BLT32, MBLT64, CBLT32/64, 2eVME, 2eSST, Multi Cast Cycles
- Transfer Rate: 60 MB/s (MBLT64), 100 MB/s (2eVME), 160 MB/s (2eSST)
- Sequential and random access to the data of the Multi Event Buffer
- The Chained readout allows to read one event from all the boards in a VME crate with a BLT access

Optical Link

- CAEN proprietary CONET protocol
- Transfer Rate: up to 80 MB/s
- Daisy Capability: up to 8 ADC modules per single optical link by A5818 Controller or A4818 Adapter

TRIGGER AND EVENT ACQUISITION

Triggered Mode

All the channels fire simultaneously upon a global trigger generated by the Central Logic Unit receiving the trigger source signals; a zero suppression function is available.

Trigger Sources

- Software by register writing
- External upon the leading edge of The TRG-IN signal (TTL/NIM)
- Local (self-trigger) upon the channel discriminator with programmable threshold

Trigger Timestamp – Waveform Rec. firmware

- Resolution: 16 ns
- Counter range: 31 bits (default); extendable to 48-bit by firmware
- Full-scale range: ~ 17 s @31-bit

SYNCHRONIZATION

Clock Generation

By default, the Digitizer’s main clocks are generated upon a 50MHz reference frequency that can optionally be internal (50MHz local Oscillator) or external (CLK-IN). Onboard programmable PLL allows locking to different external frequencies.

CLK-IN/CLK-OUT Connector

- Reference clock differential signal
- 2.54mm 3-pin AMPMODU Mod II male connector
- CLK-IN: AC-coupled LVDS, ECL, PECL, LVPECL, CML (Zdiff = 100 Ω)
- CLK-OUT: LVDS

Clock Synchronization

Default 50MHz frequency distributed by:

- Fan-in into CLK-IN (**DT4700**)
- CLK-IN/CLK-OUT Daisy chain with sw programmable CLK-OUT delay shift

PLL programming files for supported custom frequencies can be generated and loaded by the CAEN Toolbox software.

Data Synchronization

Programmable Busy/Veto logic on differential LVDS I/O, or single-ended NIM/TTL I/O for event building.

Run Synchronization (Acquisition Start/Stop)

Optionally, by Daisy chain or fan-in propagation through differential LVDS I/Os, or single-ended NIM/TTL I/O.

Trigger Distribution

TRG-IN/TRG-OUT NIM/TTL LEMO I/O (global trigger) or LVDS I/O (global or local trigger).

FPGA

Altera Cyclone III EP3C16

CAEN FIRMWARE

Waveform Recording Firmware (Freeware)

Designed for waveform recording.

Upgrades (Free)

Web available CFA files for Waveform Recording firmware upgrade through the CAEN Toolbox software, via VMEbus or Optical Link.

SOFTWARE

Readout Software for Waveform Rec. Firmware (Freeware)

- **CAEN WaveDump**: Digitizer 1.0 series support, single-board management, user-customizable

SDK and Tools (Freeware)

General-purpose libraries (C/Python, LabVIEW) with demo samples for host Windows® and Linux® PC.

ENVIRONMENTAL

- **Environment:** Indoor use
- **Operating Temperature**: 0°C to +40°C
- **Storage Temperature**: -10°C to +60 °C
- **Operating Humidity:** 10% to 90% RH non condensing
- **Storage Humidity:** 5% to 90% RH non condensing
- **Pollution Degree:** 2
- **Overvoltage Category:** II
- **EMC Environment:** Commercial and light industrial
- **IP Degree:** Enclosure (desktop models), not for wet location

REGULATORY COMPLIANCE

- EMC: CE 2014/30/EU Electromagnetic Compatibility Directive
- Safety: CE 2014/35/EU Low Voltage Directive

POWER CONSUMPTIONS

+5V: 6.5 A (Typ.)

+12V: 0.2 A (Typ.)

-12V: 0.3 A (Typ.)

Ordering Options

Code	Description	
WVX1761CXAAA	VX1761C - 2 Ch. 10 bit 4 GS/s Digitizer: 57.6MS/ch, EP3C16, SE	RoHS
WVX1761XAAAA	VX1761 - 2 Ch. 10 bit 4 GS/s Digitizer: 7.2MS/ch,EP3C16, SE	RoHS

Accessories

AI2700

Optical Fiber Series

A316

Cable assembly 2.54mm 2-pin header female - 5 cm

A952

Cable assembly 2.54mm 34 pin female to 2.54mm 34 pin female - 50 cm

A318

Adapter for Clock signal FISCHER S101A004 male to 3-pin AMPMODU IV female – 10 cm

A319B

Clock cable assembly from Digitizer Series 1.0 to Digitizer Series 2.0 - 20cm

DT4700

Clock Generator and FAN-OUT

A654

Cable assembly LEMO 00 male to MCX male – 1 m

A954

Cable assembly 2.54mm 34 pin female to two 2.54mm 16 pin female - 50 cm

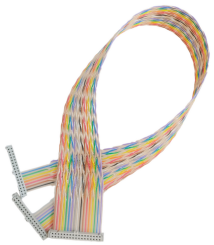
A659

Cable assembly BNC male to MCX male – 1 m

A317

Cable assembly for Clock distribution 3-pin AMPMODU IV female terminations – 18 cm / 25cm

A953



Cable assembly 2.54mm 34 pin female to two 2.54mm 34 pin female – 50 cm

Related Software

CAEN Toolbox

Multi-Functional Software Suite for the Upgrade of Front-end Boards, Bridges and Power Supplies

WaveDump

Readout Application for CAEN Digitizer 1.0

Related Firmware

D-WAVE

Digitizer Waveform Recording Firmware

Related Software Libraries

CAENDigitizer Library

Library of functions for CAEN Digitizers high level management

CAENComm Library

Interface library for CAEN Data Acquistion Modules

Related Products

VX4718

VME to USB 3.0/Ethernet/Optical Link Bridge

VME8008X

4U 8 Slot VME64X Mini Crate

VME8200

9U 21Slot VME64X Enhanced Crate series

µ-crate

Desktop single-slot VME64X Crate

VME8004X

2U 4 Slot VME64X Mini Crate

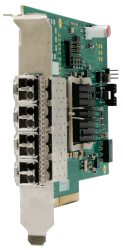
VME8100

8U 21 Slot VME64/64X Enhanced Crate Series

VX3718

VME64 to USB 2.0/Optical Link Bridge

A5818



CONET2 Controller based on PCI Express Gen 3 interface

DT5761

1 Input Channel 10 bit 4 GS/s Digitizer

V1761

2 Input Channel 10 bit 4GS/s Digitizer

A4818

USB 3.0 to CONET2 Adapter

Gallery


CAEN
DTACK
CLK IN
CLK OUT
GND
TRG OUT
TRG IN
S IN
TTL
NIM
LINK
MON / Σ
CH1

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