CAEN
Tools for Discovery

DT5560SE

32 Channels 14-bit 125 MS/s Open FPGA Digitizer

KEY FEATURES

- 32 channels, 14-bit @125 MS/s Digitizer
- Handy **Desktop** form factor
- Based on powerful Xilinx Zynq-7000 SoC with **open FPGA**
- Fully supported by **SCI-Compiler** for easy FPGA programming
- Ideally suited to readout **PMTs and Position Sensitive detectors** in **R&D/Lab development** stage
- **32 Single-ended** analog inputs on LEMO connectors
- **Programmable analog frontend**
- **[x1:x100] analog gain,** adapting to many HEP and nuclear spectroscopy detectors
- Board-to-board **synchronization** with a single CAT5e cable.
- Configurable digital I/Os to interface with external systems
- Maximum **flexibility**: USB3.0, Ethernet, and Optical Link connectivity , to support remote management as well as extreme fast data flow
- **2.4" touch screen display** for quick configuration and status control
- **Web Interface** for quick board start-up
- Default firmware for trapezoidal filter PHA and waveform recording
- Open-source SCI-55x0 Readout Software

Supported by SCI-COMPILER CAEN

High Energy Physics

Multichannel Spectroscopy

Lab R&D

DESCRIPTION

The DT5560SE is a Desktop, 32 Channel, 14-bit 125MS/s Waveform Digitizer which features an **Open FPGA** format which offers the user vast programmable data processing capabilities

The DT5560SE Open FPGA Digitizer is ideally suited to readout detectors commonly used in HEP and nuclear spectroscopy, exploiting the handy form factor for R&D and prototyping in a laboratory**.** By taking advantage of the powerful SoC architecture the user can quickly and easily design **custom logic and pulse processing algorithms** on the open FPGA, as well as develop middleware/software which perfectly matches of the application of interest. No expertise in VHDL/Verilog is required for the user to utilize this powerful tool.

The board can simultaneously manage **digital** (LVDS, NIM, TTL) and **analog** signals, thus supporting the implementation of a wide range of functionalities required by physics experiments: Signal Digitization, Complex Trigger Logic, Pulse Height Analysis with MCA capabilities, Time Tagging, Pulse Shape Discrimination, etc. The DT5560 features single-ended analog inputs on LEMO connectors and an advanced programmable input stage with different possible gain and offset, suitable to adapt to a wide range of detectors.

Critical to the DT5560SE design is an **open-FPGA** architecture. Thanks to **SCI-Compiler** software, users can combine several processing blocks in a block diagram, supporting the quick and simple development of firmware algorithms critical to data processing. In few clicks, and without the knowledge of any FPGA programming language, it is possible to implement Pulse Height Analysis (PHA), highly accurate event timing and timestamping (TDC), mathematical operations (including data fitting), Pulse shape discrimination (PSD), and much more.

Free and open-source **SCI-55x0 readout software** is also provided. This open-source demo software is designed to manage the standard pulse height analysis firmware implementing energy measurements using a trapezoidal filter together with waveform recording.

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TECHNICAL SPECIFICATIONS

GENERAL	**Form Factor** Desktop module 257x102x331 mm3 (WxHxD)		
POWER CONSUMPTION	300 mA @ 220 Vac (Typ.)		
ANALOG INPUT	**Channels** 32 single-ended inputs on LEMO		
	Impedance 50 Ω/1 kΩ programmable **Bandwidth** 60 MHz Programmable DC offset adjustment on each input in the full scale range	**Analog Coarse Gain** [x1:x100]	**Full Scale Range** [0.015 V_{pp}: 1.5 V_{pp}]
DIGITAL I/Os	**USER IO 0…2 (LEMO)**		
	Programmable Digital I/Os, function stated at firmware level. Can be used as Trigger, Start, Busy Single-ended, Zin / Rt = 50 Ω		
DIGITAL CONVERSION	**Resolution** 14 bits	**Sampling Rate** 125 MS/s Simultaneously on each channel	
CLOCK GENERATION	**125 MHz ADC clock** Clock sources: internal/external Internal 25 MHz oscillator External 25 MHz – USER IN 0 or SYNC connector		
TRIGGER	**Trigger Source** *Internal/External*: managed by the default firmware *Complex trigger logic*: implementable by the user on the open FPGA	**Trigger Propagation** Through USER I/Os and Sync Connector **Trigger Time Stamp** *Default FW*: 32-bit counter, 8 ns resolution, 26-day range; *Custom FW*: defined by the firmware design	
SYNCHRONIZATION	**Clock Propagation** USER I/Os connectors SYNC Connector	**Acquisition Synchronization** Through programmable LEMO Through dedicated SYNC Connector **Sync connector allows to cascade multiple units and synchronize them with a single standard CAT5e cable**	
FPGA	**Open FPGA** 1x Xilinx Zynq-7000 SoC Z-7030		
MEMORY	1 GByte of memory for list readout on each SoC Up to 8kS/ch for simultaneous waveform readout		
COMMUNICATION INTERFACE	**Ethernet** 1Gbps **Optical Link** Slots for 2 x 10Gbps SFP+ transceivers (communication protocol not implemented by default) **USB 2.0** 1x mini-USB	The different readout interface allows to integrate the DT5560SE in existing experimental environment.	
FIRMWARE	**Default** -Waveform recording and Pulse Height Analysis - Ethernet/USB communication	**Custom** Use SCI-Compiler to develop your own firmware!	
FIRMWARE UPGRADE	Firmware can be upgraded via Ethernet, mini-USB or JTAG mini-USB debugger (on-the-fly)		
SOFTWARE	**SCI-55X0 Readout Software** to manage the default firmware **SCI-Compiler** for custom firmware development		

Ordering Option

Ordering code	Description
WDT5560SEXAA	DT5560SE 32 Ch. 14 bit 125 MS/s Digitizer single-ended (SciCompiler SW555 included)

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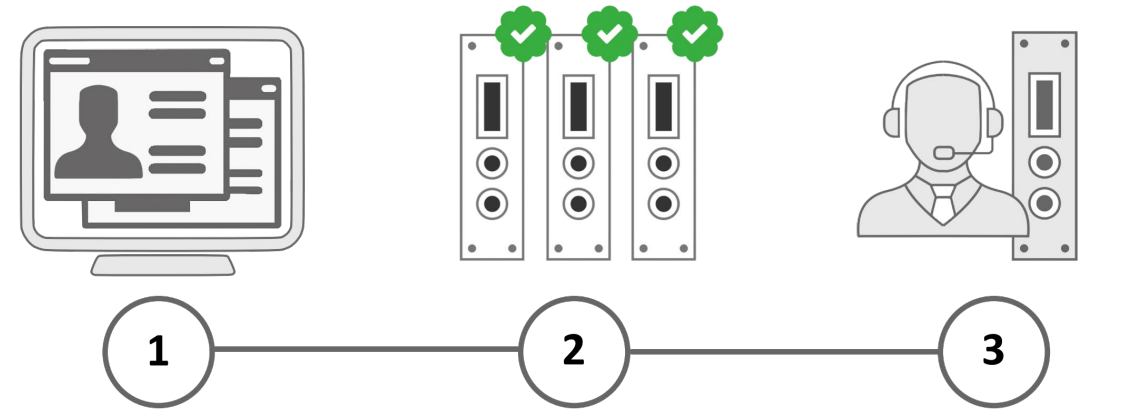

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