CAEN
Tools for Discovery

2740/2745

Digitizer Family

64-Channel 16-bit 125 MS/s

open FPGA

16bit 125MS/s

DESKTOP RACK VME Form Factor

1/10 GbE

USB 3.0

VGA

WEB INTERFACE

The new generation of CAEN Digitizers: Open FPGA and Digital Pulse Processing algorithms for high-density channel experimental setups!

Overview

The 2740/2745 Digitizer is a 64-channel digital signal processor for radiation detectors available in VME64 (V2740/V2745), VME64X (VX2740VX2745), and Desktop (DT2740/DT2745) form factor. It offers not only waveform digitization and recording but also Multi-Channel Analysis for nuclear spectroscopy using Silicon strip, segmented HPGe, Scintillation detector with PMTs, Wire Chambers, and others. The powerful computational resources of the embedded CPU make the 2740/2745 suitable for different kind of algorithms of pulse processing, from pulse height analysis (PHA) to constant fraction discrimination (CFD), charge integration and pulse shape discrimination (PSD), to be applied independently on each of the 64 channels. While the 2740 Digitizer is fixed-gain, the 2745 offers a software programmable analog gain up to x100.

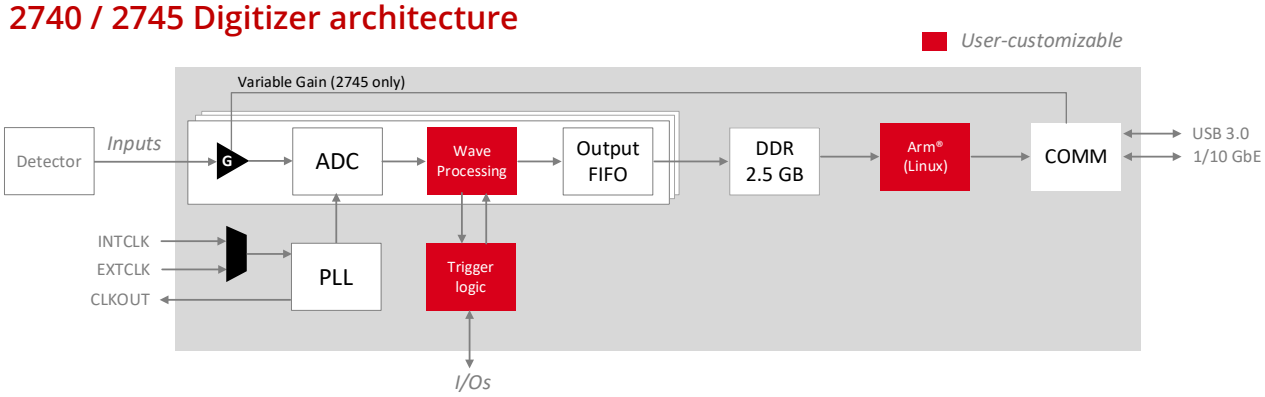
Highlights

- High channel density: 64-channel, 125MS/s 16-bit ADC with individual DC offset adjustment.
- Available in VME64, VME64X and Desktop form factors.
- SW selectable analog gain (2745 only)
- Front panel readout via USB-3.0 or 1/10Gb Ethernet
- Up to 42 ms of continuous wave recording per channel in DDR4 memories
- Onboard Zynq® UltraScale+™ MPSoC integrating an Arm®-based CPU running Linux®
- Open FPGA architecture fully supported by Sci-Compiler tool
- Digital pulse processing and waveform recording of 64 independent detectors
- Advanced waveform readout modes with Zero Length Encoding (ZLE)
- Originally designed for Dark Matter Physics applications
- Suitable for Si strip, segmented HPGe, scintillation detectors, and others
- High-resolution Nuclear Spectroscopy: multiport MCA operating in PHA, PSD modes
- Digital CFD for sub-ns timing measurements
- Multi-board synchronization facilitated by front panel programmable digital I/Os
- Front panel DAC output programmable for signal inspection, pulse generation, majority level

Software

- GUI-based readout software available for multiparametric spectroscopy (CoMPASS) or waveform recording (WaveDump2)
- Firmware/software generator and compiler for the Open FPGA (Sci-Compiler), eliminating the need for FPGA programming skills
- Libraries (FELib) and demo codes available for software customization

2740 / 2745 Digitizer architecture

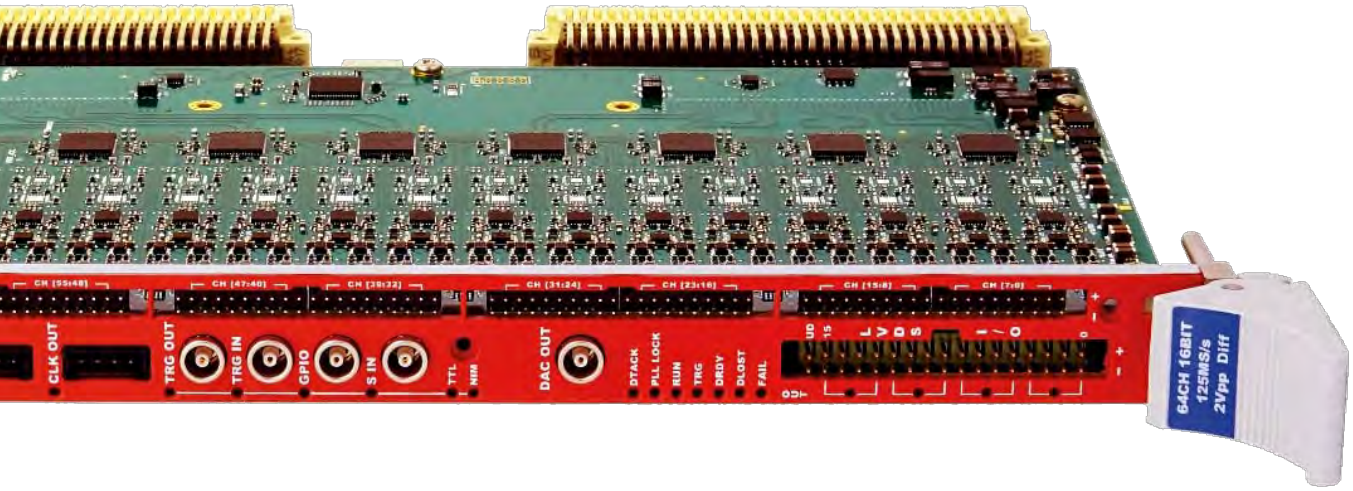


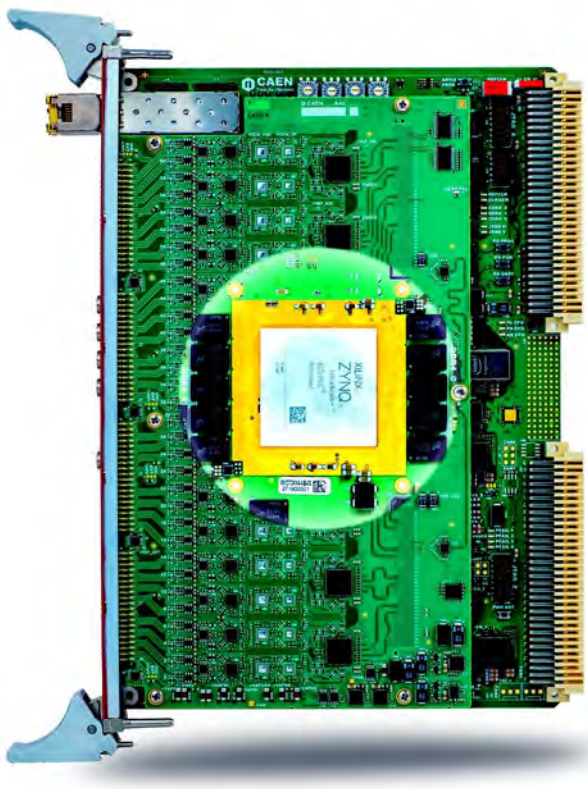
Data Acquisition

CAEN digitizers support multiple data acquisition modes, implemented as distinct FPGA firmware solutions, making them adaptable to a wide range of radiation detection applications in Nuclear Physics. The CAEN 2740/2745 Digitizer Family features 64 single-ended (on 2740B/2745B versions) or differential channels, each one capable of digitizing detector signals with a 16-bit ADC at 125 MS/s. The data acquisition is driven by the trigger signal generation and the identification of a Region of Interest (ROI), defined in terms of samples or time duration. Trigger sources can basically be either local (channel self-trigger), or external, or software. Once acquired, the digitized data is processed in the FPGA, stored in high-speed memory by events including Trigger ID/Timestamp tag, and then transferred via high-bandwidth communication interfaces for further analysis. The Digitizer operates in different acquisition modes, designed to balance throughput, latency, and data efficiency based on experimental needs.

Triggered mode: All channels acquire data simultaneously upon a global trigger generated by a Central Logic Unit that processes the local triggers received from the channels. Optionally, the external and software trigger can also be the source for the global trigger. Zero suppression algorithms can be applied to remove non-significant data and reduce the readout payload.

Streaming readout mode: Each channel identifies the ROI autonomously. The channel self-trigger is used to acquire data independently on the other channels. This mode implements automatic zero suppression (not fired channels are not acquired), it maximizes acquisition rates, and it is ideal for applications requiring real-time parameter extraction. Coincidence/anticoincidence logic can be configured to validate the event acquisition upon the combination of the local trigger with other local triggers and/or external I/Os.





FPGA & Arm Processor

The CAEN 27xx Digitizer Family has been equipped with a Xilinx Zynq UltraScale+ MPSoC including FPGA and Arm-based processor running Linux.

In the 27xx architecture, specific functional FPGA blocks are open for custom firmware solutions. Users can control the data output information and implement complex trigger logics using I/O signals to validate or discard the events.

Users can also automatize processes programming custom software routines in the Linux operating system hosted on the embedded Arm processor.

Synchronization

Multi-board synchronization of 27xx digitizers can be achieved by front panel cabling optimization (e.g. both clock and sync signals sent on CLK-OUT / CLK-IN), or by P0 backplane[1].

[1] *Customization available on request*

Connectivity

Multi-interface options are available on the front panel: USB-3.0 with maximum tested transfer rate of 280 MB/s; 1/10 Gb Ethernet with up to 1100 MB/s[2] measured transfer rate for 10G UDP.

[2] *See application note: AN12165 - Benchmarking Streaming Readout Performance of CAEN Digitizers.*

Firmware & Software

The 2740/2745 Digitizer Family can be operated upon both pre-configured firmware developed by CAEN and custom user-generated firmware, offering flexibility for a wide range of applications. More than a firmware can be simultaneously stored in the Digitizer FLASH memory and quickly activated if necessary.

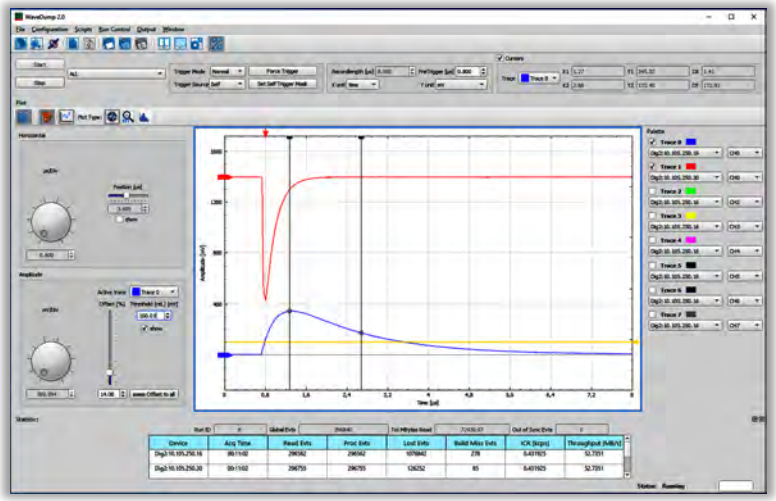
CAEN provides ready-to-use firmware solutions, optimized for specific acquisition and processing needs:

- Scope firmware: based on full waveform recording in triggered acquisition mode. Zero suppression function is available to reduce unnecessary data readout.
- DPP-PHA Firmware: Implements Digital Pulse Processing for the pulse shape analysis. Physical parameters such as pulse height, charge and timestamp are extracted from waveforms acquired in streaming readout It is yet possible to save both raw waves and parameters.
- DPP-PSD firmware: implements Digital Pulse Processing algorithms of charge integration and pulse shape discrimination. Physical parameters like energy, timestamp and PSD are extracted from the waveforms acquired in streaming readout mode. CFD function is available for fine timestamp.
- DPP-ZLEPLUS Firmware: Implements Digital Pulse Processing algorithms for the Zero Length Encoding. Data reduction is so achieved on the recorded waveforms while they are acquired in triggered mode.

Dedicated CAEN software tools are available to manage the firmware solutions:

- WaveDump2 works with Scope Firmware, providing a user-friendly interface for waveform acquisition and real-time data visualization.
- CoMPASS is compatible with DPP-PSD Firmware, allowing multiparametric data acquisition, real-time PSD analysis, and event-based visualization.
- FELib (Front-End library) facilitates users needing custom software development. It is a comprehensive C/C++ API for direct interaction with the digitizer hardware, enabling custom DAQ implementations with full control over data acquisition parameters and processing workflows.

For users requiring custom acquisition and processing, the Open FPGA architecture enables firmware customization through Sci-Compiler. This versatile graphical tool not only makes users capable of producing personalized firmware solutions without need of FPGA programming language skills but also generates the drivers and libraries and offers graphical tools to develop custom DAQ software.



www.caen.it/products/wavedump2/

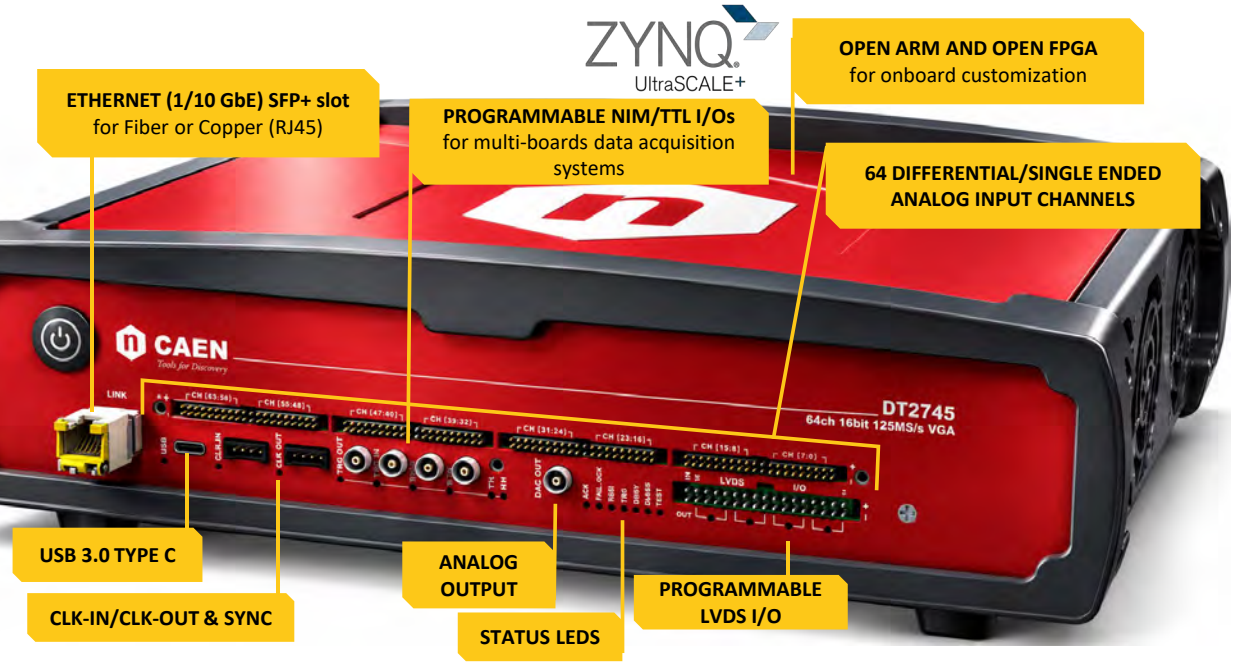
WaveDump2 software

- Waveform recording application
- Multi-board management
- Simultaneous plot of waveforms from up to 8 input channels
- Flexible and easy configuration of channel and trigger settings
- Runtime FFT analysis

WaveDump2 is a C++ software designed to support the Digitizer Series 2.0, running the scope firmware for waveform recording provided by CAEN. Developed using the Qt cross-platform application development framework, this software offers an advanced and user-friendly configuration GUI. It provides a comprehensive range of tools and functionalities to manage various hardware parameters, from basic settings to more specific ones. Configuration settings can be conveniently stored in or loaded from configuration files. The software also facilitates data acquisition from multiple boards and synchronized systems through a dedicated toolbar. The collected data can be saved in ASCII or binary file formats for offline analysis.

The program includes a plot section that functions as an 8-channel digital oscilloscope emulator. This tool allows users to review acquired waveforms, fine-tune device settings, and troubleshoot potential issues. The oscilloscope interface features cursors for on-screen measurements, as well as marker lines to indicate the trigger position and trigger threshold level. Traces can be individually enabled or disabled, and a legend is provided to easily identify displayed signals. The graphical tool offers zooming controls in both the vertical and horizontal directions. Basic processing capabilities, such as FFT (Fast Fourier Transform) and samples histogramming, are available in real-time.

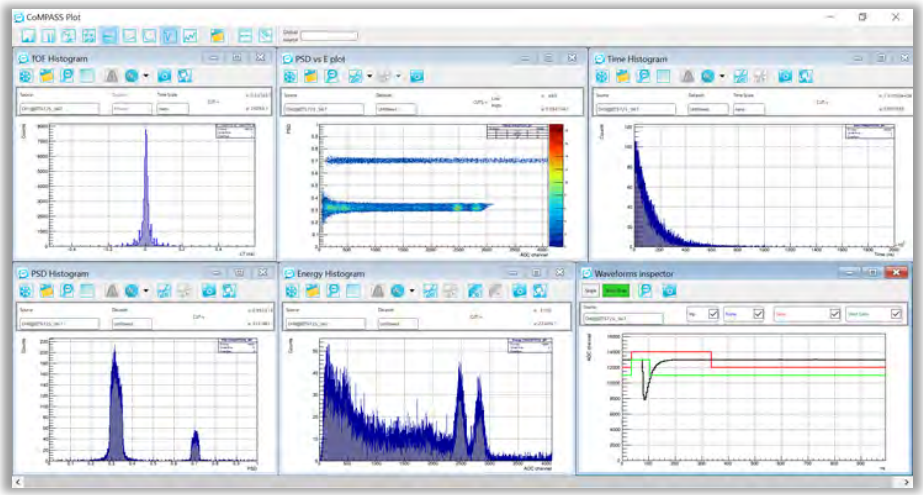
WaveDump2 is compatible for Windows® and Linux® platforms.



www.caen.it/products/compass/

CoMPASS multiparametric software

- Simultaneous plot of waveforms, Time, Energy, PSD, and TOF spectra
- Online filtering (Time, Energy, PSD)
- Multi-board management
- Advanced data saving
- ROOT format data saving



CAEN Multi-PArameter Spectroscopy Software (CoMPASS) is the data acquisition (DAQ) software designed for both Digitizer Series 1.0 and 2.0, running the DPP (Digital Pulse Processing) firmware provided by CAEN. It enables Multiparametric Data Acquisition for Physics Applications, where detectors can be directly connected to the digitizers/MCAs inputs, allowing simultaneous acquisition of energy, timing, and PSD (Pulse Shape Discrimination) spectra.

CoMPASS software offers a user-friendly interface designed to manage the acquisition process using all the CAEN DPP algorithms. It provides easy configuration of acquisition parameters and allows up to six different plots and histograms to be displayed simultaneously. CoMPASS can handle multiple boards and enables straightforward synchronization of multiboard systems. Some of the key features of CoMPASS include event correlation between different channels (both in hardware and software), energy, PSD, and time selections, calculation and display of acquisition statistics (trigger rates, data throughput, percentage of discarded events due to selections, etc.), basic mathematical analysis of recorded spectra (ROI selection, background subtraction, peak fitting, etc.), saving output data files (raw data, lists, waveforms, spectra), and offline processing using saved files with different processing parameters.

For users familiar with the ROOT Analysis Framework, CoMPASS provides the option to save output files (lists, waveforms, and spectra) in the ROOT TTree format, allowing easy post-processing with customized analysis code .

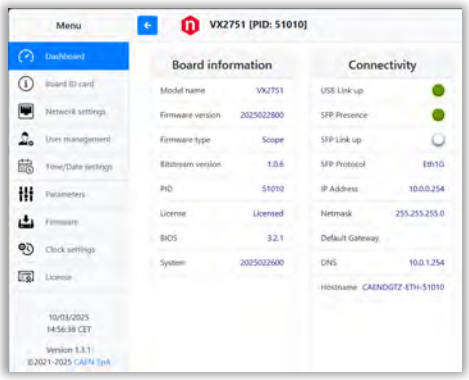
CoMPASS is available for Windows® and Linux® platforms.

www.caen.it/products/caen-toolbox/

CAEN ToolBOX is a software utility designed to upgrade and manage the firmware on the 27xx Digitizer Family. This highly versatile software suite supports a wide selection of CAEN devices, including front-end boards, Digitizer 1.0 and 2.0 series, bridges and controllers, PLU, and power supplies. It offers a user-friendly GUI or command line application to manage onboard firmware, perform debug tests, and execute other useful functions. .

ToolBOX is available for Windows® and Linux® platforms.

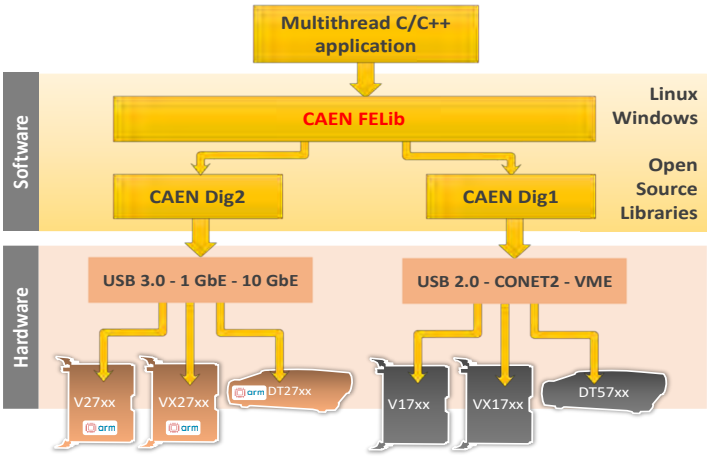
The Digitizer 27xx features an intuitive Web Interface that allows users to access key service functionalities directly from a web browser, without requiring additional software. This interface enables real-time hardware status monitoring, providing visibility on operating parameters and error notifications. Users can configure and manage network connectivity settings, either by manually assigning an IP address or using DHCP for automatic allocation. The Web Interface also supports firmware management, allowing seamless upgrades and selection of available versions directly from the control panel. Additionally, it offers advanced configuration options, including PLL management, enabling precise synchronization of the digitizer's internal clock. Access is available via USB or Ethernet, with credential-based authentication ensuring different authorization levels for administrators and standard users.

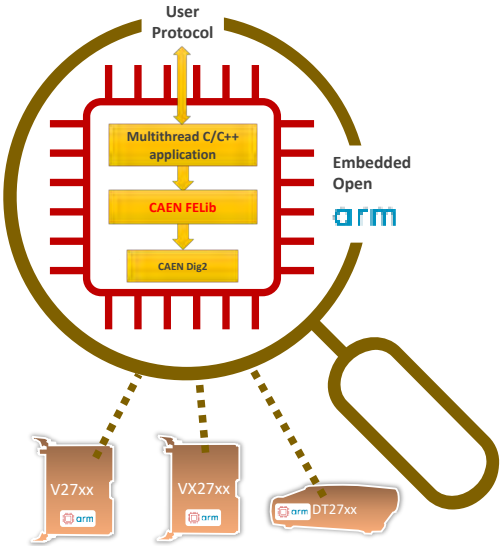


www.caen.it/products/caen-felib-library/

CAEN FELib Library

- Set of functions designed for controlling and utilizing Digitizers 2.0 (2740, 2745, 2730, and 2751 family).
- Available in C/C++ and Python for both Windows and Linux operating systems.
- Distributed as an open-source software under the GNU Lesser General Public License 3.
- Provides multithread support for enhanced performance.

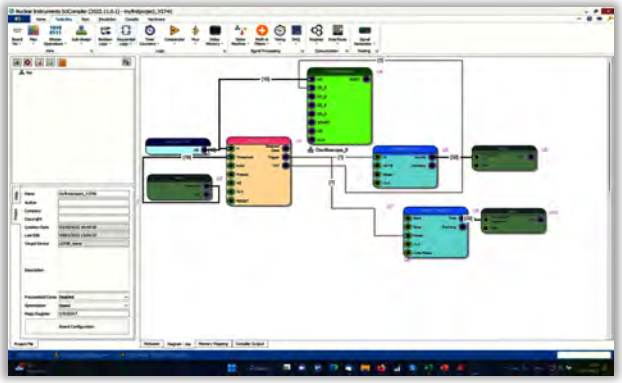




CAEN Waveform digitizers x27xx introduce a new way of accessing the firmware parameters, providing an abstraction of the registers in the form of library parameters that are much easier to understand and use.

This new way is designed to simplify the life of those users who need to build their own DAQ system and software and access the digitizer firmware parameters. CAEN FELib can be used to control and acquire data from the new generation of CAEN digitizers. This library is only an interface and does not include support for any digitizer family. To use a digitizer, the user must also install the corresponding CAEN Digx library.

FELib is compatible for Windows® and Linux® (x86 and Arm) platforms.



www.caen.it/products/sci-compiler/

Sci-Compiler

- Block-diagram-based programming tool for CAEN Open FPGA boards
- Designed to make FPGA access easier, even for non-expert programmers
- Offers 100+ advanced signal processing blocks for Physics and Nuclear Engineering
- Provides Remote Customization Service for compilation and simula-

Sci-Compiler, short for Scientific Compiler, is a graphical software tool designed to simplify and expedite the implementation of firmware in physics applications for open FPGA CAEN boards. By creating a block diagram, the software can automatically generate firmware that can be directly deployed on compatible hardware. This means that even users without expertise in VHDL/Verilog programming can create their own firmware code. It is a unique tool that generates and compiles FPGA code, downloads it onto the target device, and allows real-time data acquisition on a host computer.

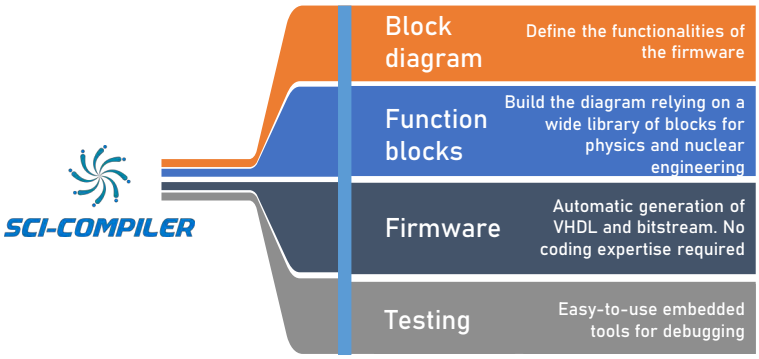
The Sci-Compiler tool includes over 100 virtual blocks that implement complex functions commonly used in physics applications. These functions include waveform recording, logic gates, TDC (Time-to-Digital Converter), spectrum reconstruction, pulse shape discrimination, and more.

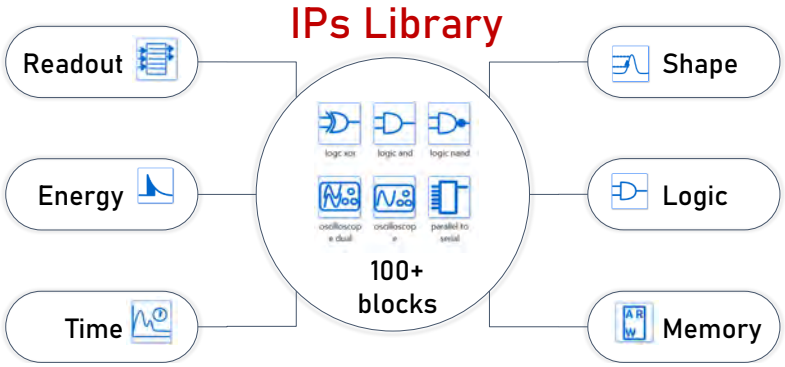
Sci-Compiler is currently available for Windows® platforms.

Sci-Compiler is a software tool that simplifies and accelerates the R&D phase. It allows users to create a diagram by placing and connecting different blocks (e.g. oscilloscope, TDC, MCA, charge integration, etc.) that represent the desired functions. Sci-Compiler then automatically generates and deploys a VHDL code to the FPGA that implements those functions.

This way, even users who are not familiar with VHDL/Verilog can write their own firmware code by focusing on the functional blocks of their application.

In addition, Sci-Compiler provides a Software Development Kit (Sci-SDK) for Windows and Linux that is compatible with the custom firmware for any supported board. The SDK consists of drivers, libraries and example codes in C++ and Python, making it easy to create a custom DAQ software that can run on Windows or Linux.





The Sci-Compiler software enables the development of both purely digital applications, using blocks such as logic gates, scaler, state machine, and analog processing applications, such as custom Multichannel Analyzers, charge integration, Pulse Shape Discrimination, Waveform recording with custom trigger logic, and many more.

Sci-Compiler is capable of automatically generating VHDL firmware code that implements the functions specified in the block diagram.

The compilation process is made highly accessible through the optional Remote Customization Service, which allows you to generate an operating firmware even if you don't have a complete FPGA compiler software installed on your local PC. This greatly simplifies the software setup. By utilizing the Remote Customization Service, Sci-Compiler handles the addition of hard-coded components to your project that remain consistent in each firmware, and generates the final firmware file. This file is then ready to be deployed onboard. CAEN provides the Remote Customization Service and Yearly Upgrade Plan to deliver a high-quality software product with the necessary flexibility to meet the users' requirements.

Sci-Compiler license

A User Account-Based License allows access to SCI-Compiler through individual user accounts. Each user must have a unique account to use the software, and th license is tied to the user's credentials rather than a physical device or hardware key.

Runtime license

Using a single Sci-Compiler license, it is possible to compile and deploy firmware for multiple compatible boards that have been activated through a runtime license. A different runtime license is needed for each board.

Remote Customization / Upgrade

Remote customization service allows to generate the firmware code with minimal local resources

Stay up-to-date with the newest Sci-Compiler features by subscribing the yearly upgrade service

www.sci-compiler.com

Ordering Option

Description	Code
SW555 - Sci-Compiler PRO License	WSW555PROXAA
SCI-Compiler runtime license for Digitizer 2.0 series	WSW55RUNTIME
1 year remote customization service + upgrade for Sci-Compiler	WSW55RCSXAAA
5 years remote customization service + upgrade for Sci-Compiler	WSW55RCSX5YA

Technical Specifications

General Features

Analog Inputs		
Number of Channels	64	Differential on 274x version / Single-ended on 274xB version
Impedance	Single ended - 50 Ω (default) - 10 kΩ (personalization)	Differential) - 100 Ω
Connector	Four 2mm 40-pin header male Input adapters available	
	2740	2745
Full scale range (FSR)	2 V_{pp}	4 V_{pp} ÷ 0.04 V_{pp}
Individual Offset adjustable in the range	±1.25 V	± 2.5 V
Bandwidth (-3 dB)	50 MHz	20 MHz guaranteed for all Gain settings
Gain	x1	x1 ÷ x100 Software programmable In steps of 0.5 dB independently on each 16-channel group [15:0], [31:16], [47:32], [63:48]
ICMR (Input Common-Mode Range) Differential models only	± 8 Vdc referred to GND	± 12 Vdc referred to GND
Digital Conversion / System Performance		
Resolution	16 bits	
Sampling Rate	125 MS/s (simultaneously on each input). Scalable by 2^n decimation factor, n = 1 to 10 (Scope firmware only)	
	2740	2745
ENOB	11.7 (Typ.)	12.0 (Typ. @5 MHz, -3dB, Gain x1)
RMS	3.9 LSB (~ 120 μV) typical	3.6 LSB RMS (@Gain x1)

Digital I/O and Analog Output		
CLK-IN	Two differential pairs: - CLK: reference clock signal - SYNC: synchronization signal (start/stop, T0, etc.)	AC-coupled LVDS, ECL, PECL, LVPECL, CML Zdiff = 100 Ω 2.54 mm 4-pin AMPMODU Mod II male connector
CLK-OUT	Same functionalities as CLK-IN Daisy chainable in multi-board synchronization with sw programmable delay shift	LVDS 2.54 mm 4-pin AMPMODU Mod II male connector
TRG-IN/TRG-OUT/GPIO/S-IN	General-purpose I/Os Software programmable (trigger, gate, veto, busy, etc.) - TRG-IN/S-IN internally terminated with 50 Ω (Zin = 50 Ω) - TRG-OUT requires Rt = 50 Ω - GPIO as Input must be terminated with 50 Ω - GPIO as TTL Output requires Rt = 50 Ω - GPIO as NIM Output requires Rt = 50 Ω or 25 Ω	Single-ended TTL/NIM LEMO 00 female connector
LVDS I/O	16 differential pairs Software programmable I/O (individual self-trigger outputs, trigger validations, Veto, Busy, Start, Stop, Pattern Input, etc.)	LVDS Zdiff = 100 Ω (when set as inputs) 2.54 mm 34-pin AMPMODU Mod II male connector
DAC OUT	DAC output for signal inspection, pulse generation, majority level 14-bit Digital-to-Analog Converter (DAC) 125 MS/s Update Rate	±1 V @ 50Ω load ±2 V @ hi-Z load Output Range LEMO 00 connector

Acquisition Memory

2.5 GB total DDR4 memory size divisible in multiple buffers.
Maximum record length: ~ 42 ms @ 125 MS/s (2-event-buffer configuration)[3]

[3] *Value referred to the Scope firmware (minimum of two buffers admitted)*

Technical Specifications (continued)

Communication Interfaces

1 GbE	Copper RJ45 or optical LC connector on SFP+ transceiver TCP/IP protocol	Transfer rate: 110 MB/s
10 GbE (Available on Request)	Copper RJ45 or LC optical connector on SFP+ transceiver UDP Protocol:	Transfer rate: 1100 MB/s[4] [4] *See Application Note: AN12165 - Benchmarking Streaming Readout Performance of CAEN Digitizers*
USB 3.0	USB-C type connector USB 3.1 GEN1 protocol	Transfer rate: 280 MB/s

Acquisition Modes

Trigger Modes	
Triggered Mode	All the channels fire simultaneously upon a global trigger generated by the Central Logic Unit receiving the trigger source signals; a zero suppression function is available
Streaming Readout Mode	Each channel autonomously identifies the ROI and uses the local trigger to get events independently on the other channels; validation logics can be configured for correlated acquisition (coincidence/anticoincidence)

Trigger

Trigger sources	- Software by register writing - External upon the leading edge of The TRG-IN signal (TTL/NIM) - Local (self-trigger) upon the channel discriminator with programmable threshold

Trigger Time Stamp	Scope Firmware	DPP firmware
Resolution:	8 ns coarse time stamp	8 ns coarse time stamp, 8 ps fine time stamp
Counter range:	48 bits	48 bits
Full-scale range:	~625 h	~78 h

Clock & Synchronization

Clock Generation	By default, the Digitizer's main clocks can be optionally generated upon from the internal 50MHz or external 62.5MHz reference (CLK-IN). Onboard programmable PLL allows locking to different external frequencies
Clock Synchronization	Typical 62.5[5] MHz frequency optionally distributed by: - fan-out to CLK-IN - CLK-IN/CLK-OUT daisy chain with sw programmable CLK-OUT delay shift [5] *Custom frequencies can be supported on request*
Run Synchronization (Acquisition Start/Stop)	Optionally, by Daisy chain or fan-out propagation through differential CLK-IN/CLK-OUT or LVDS I/O, or single-ended NIM/TTL I/O
Data Synchronization	Programmable Busy/Veto logic on differential LVDS I/O, or single-ended NIM/TTL I/O for event building
Trigger Time Stamp Reset	Optionally, by Software from start run command or Hardware from S-IN/GPIO input (Scope Firmware only)
Trigger Distribution	TRG-IN/TRG-OUT NIM/TTL LEMO I/O (global trigger) or LVDS I/O (global or local trigger)

Firmware and FPGA

FPGA	
Device	Xilinx Zynq UltraScale+ Multiprocessor System-on-Chip mod. XCZU19EG Processing System based on Quad-core Arm with 2GB DDR4 memory @2400 MT/s (Linux OS onboard) Programmable logic with more than 1100K system logic cells and 80Mbit memory
CAEN Firmware	**Developed by CAEN, stored in the on-board FLASH memory, and live rebootable by Web Interface**
DPP Firmware	Firmware implementing Digital Pulse Processing algorithms[6]: - DPP-PHA: Pulse Height Analysis - DPP-ZLEplus: Zero Length Encoding - DPP-PSD: Pulse Shape Discrimination [6] *30-minute per power cycle in Trial mode, license is required for full-time work*
Scope Firmware	Firmware for the waveform recording
Upgrades	CAEN firmware can be uploaded via Web Interface or CAEN Toolbox software (scope and DPP firmware, and their updates)

Technical Specifications (continued)

User Firmware (Open FPGA)	
SCI-Compiler	User Firmware Generator and Compiler Graphical Tool for CAEN Programmable Boards

Customizable features of the Scope FW:
- Common trigger
- Simultaneous waveform recording on 64 channels management
- Trigger logic
- Wave processing

Customizable features of the DPP firmware:
- Individual trigger and channel acquisition management
- DPP algorithm
- Trigger logic
- Event data information

Software

Readout Software
CoMPASS spectroscopy software (CAEN DPP firmware only) for Windows® and Linux®
WaveDump2 (CAEN scope firmware only) for Windows® and Linux®
SCI-Compiler (Open FPGA): Automatic generation of drivers (USB, ethernet), libraries, and demo software for Windows®
Web Interface
Firmware management (e,g. upgrades and on-the-fly selection of the firmware to run), board information, PLL and Ethernet configuration, board status monitoring, DPP license management
SDK and Tools
General-purpose C libraries with demo samples for host Windows® and Linux® PC, and embedded Arm processor

Mechanical

	V2740 / V2740B V2745 / V2745B	VX2740 / VX2740B VX2745 / VX2745B	DT2740 / DT2740B / DT2745 / DT2745B	
Form Factor	1-unit wide VME64 6U x 160 mm	1-unit wide VME64X 6U 6U x 160 mm	Desktop	Desktop-Rack
Weight	642 g	642 g	3120 g	3170 g
Dimension			341 W x 100 H x 303 L mm³ (including connectors)	19" rack mount

Environmental

Environmental	Indoor use	Pollution Degree	2
Operating Temperature	0°C ÷ +40°C	Overvoltage Category	II
Storage Temperature	-10°C ÷ +60°C	Overvoltage Category	II
Operating Humidity	10% ÷ 90% RH non condensing	EMC Environment	Commercial and light industrial
Storage Humidity	5% ÷ 90% RH non condensing	IP Degree	Enclosure (desktop models), not for wet location

Regulatory

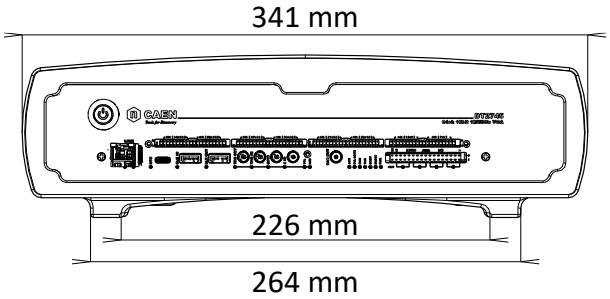
Compliance	EMC:	CE 2014/30/EU Electromagnetic compatibility Directive
	Safety:	CE 2014/35/EU Low Voltage Directive

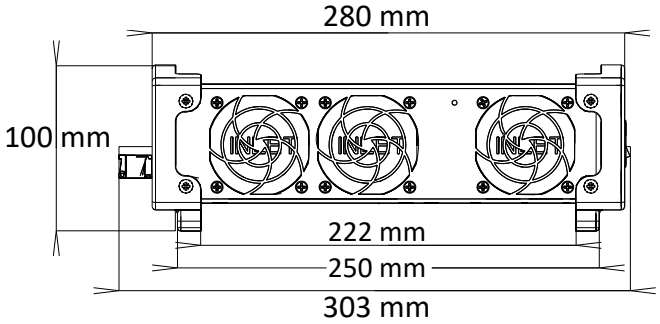
Power Requirements

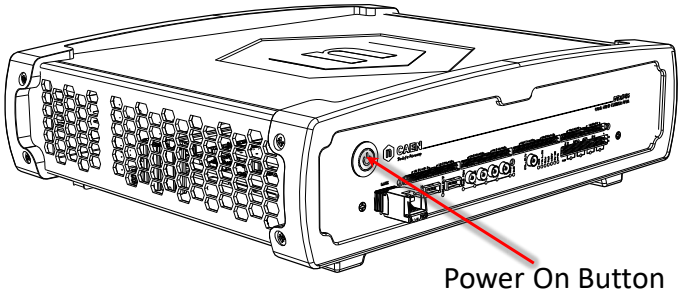
	V2740 / V2740B[7]	VX2740 / VX2740B[7]	DT2740 / DT2740B
+ 12V	1.1 A	1.1 A	n. a.
+ 5 V	6.2 A	2.7 A	n. a.
+ 3.3 V	Not used	4.9 A	n. a.
			Mains Powered (100÷240 Vac, 50÷60 Hz; Max power: 130 W)
	V2745 / V2745B[7]	**VX2745 / VX2745B[7]**	**DT2745 / DT2745B**
+ 12V	1.4 A	1.4 A	n. a.
+ 5 V	9.0 A	5.3 A	n. a.
+ 3.3 V	Not used	4.9 A	n. a.
			Mains Powered (100÷240 Vac, 50÷60 Hz; Max power: 130 W)

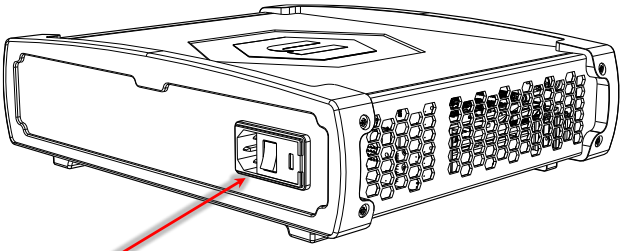
[7] *The values above are typical and preliminary, referring to a 1-GbE Scope firmware; they may vary depending on the firmware type.*

DT2740/DT2745 Mechanical Dimension

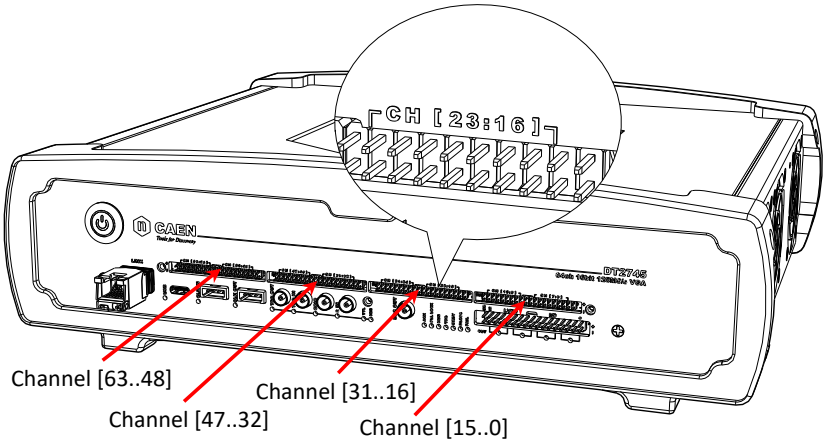


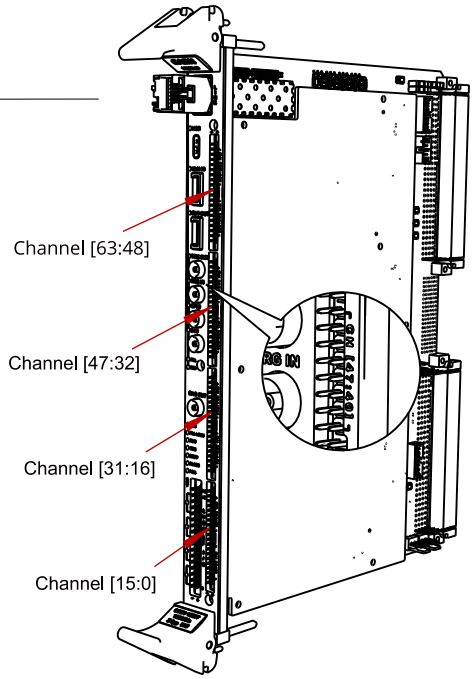




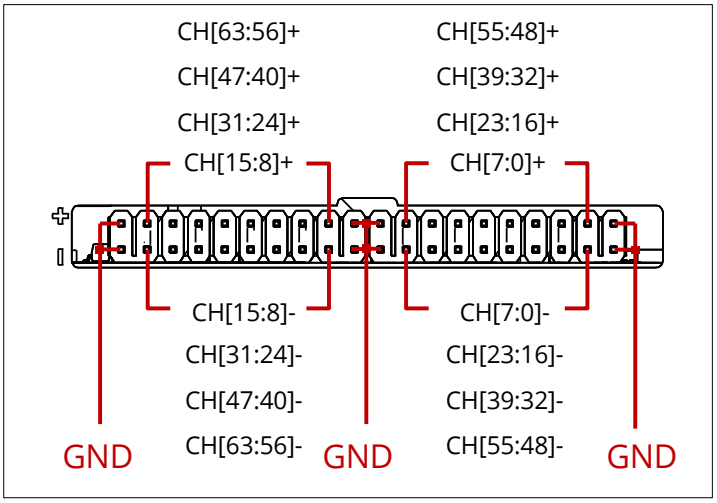


2740/2745 Analog Input Pinout

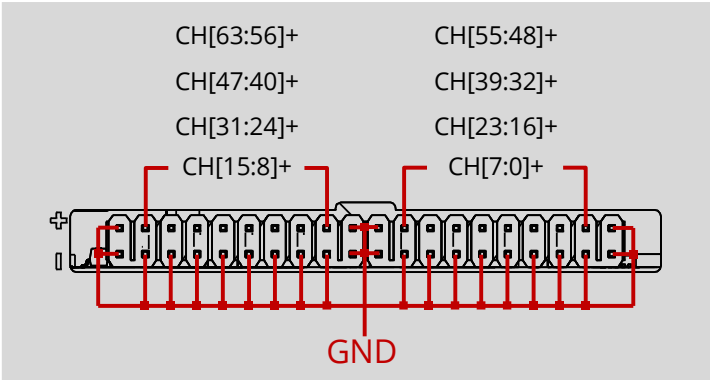




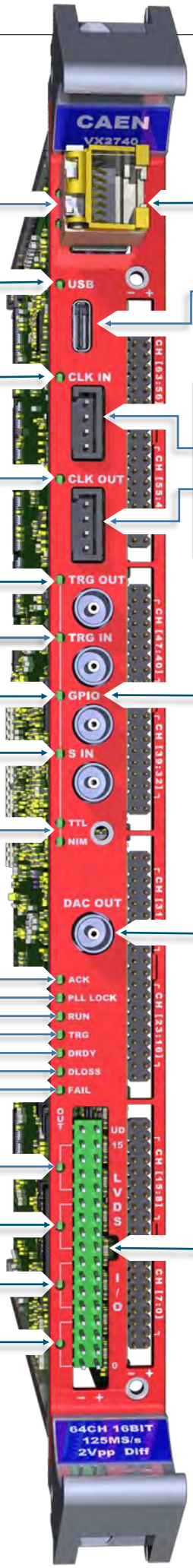
Differential (2740/2745)



Single-ended (2740B/2745B)



2740/2745 Front Panel and LED behavior



LINK Ethernet network indicator
- Ethernet link unavailable (cable off)
- Ethernet link available (cable in)
- Data activity on the ethernet link

USB USB Link Indicator
- USB link unavailable (cable off)
- USB link available (cable in)
- Data activity on the USB link

CLK IN Reference Clock indicator
- Internal clock reference enabled
- External clock reference enabled

CLK OUT Reference Clock indicator
- Reference clock propagation disabled
- Reference clock propagation enabled

TRG OUT / TRG IN / GPIO / S IN LEMO I/O level indicator
- No activity on the relevant connector
- Signal activity on the relevant connector

TTL / NIM LEMO I/O level indicator
- NIM or TTL level enabled for the 4 LEMO I/Os

ACK Readout activity indicator
- No readout access to the board through USB or Ethernet
- Read or Write access to the board through USB or Ethernet

PLL LOCK PLL lock indicator
- The PLL is not locked to the reference clock
- The PLL is locked to the reference clock

RUN Acquisition (data taking) indicator
- The acquisition is off
- The acquisition is running

TRG Accepted Trigger indicator
- The trigger is accepted

DRDY Data ready indicator
- Event/Data is present in the Output Buffer

DLOST Data loss indicator
- The trigger arrived while the board is in busy state. This trigger is rejected and the relevant event/data is lost

FAIL Board fail indicator
- A power fail, over temperature condition or PLL lock loss occurred

OUT LVDS I/O direction indicator
- LVDS I/O 4-pin group direction is INPUT
- LVDS I/O 4-pin group direction is OUTPUT

LINK Ethernet Transceiver (inserted in the SFP+ receptacle)

USB Type-C Connector

CLK-IN / CLK-OUT 2.54mm 4-pin AMPMODU Mod II male connector

CLK IN		CLK OUT	
4	SYNC_IN -	4	SYNC_OUT -
3	SYNC_IN +	3	SYNC_OUT +
2	REFCLK_IN -	2	REFCLK_OUT -
1	REFCLK_IN +	1	REFCLK_OUT +

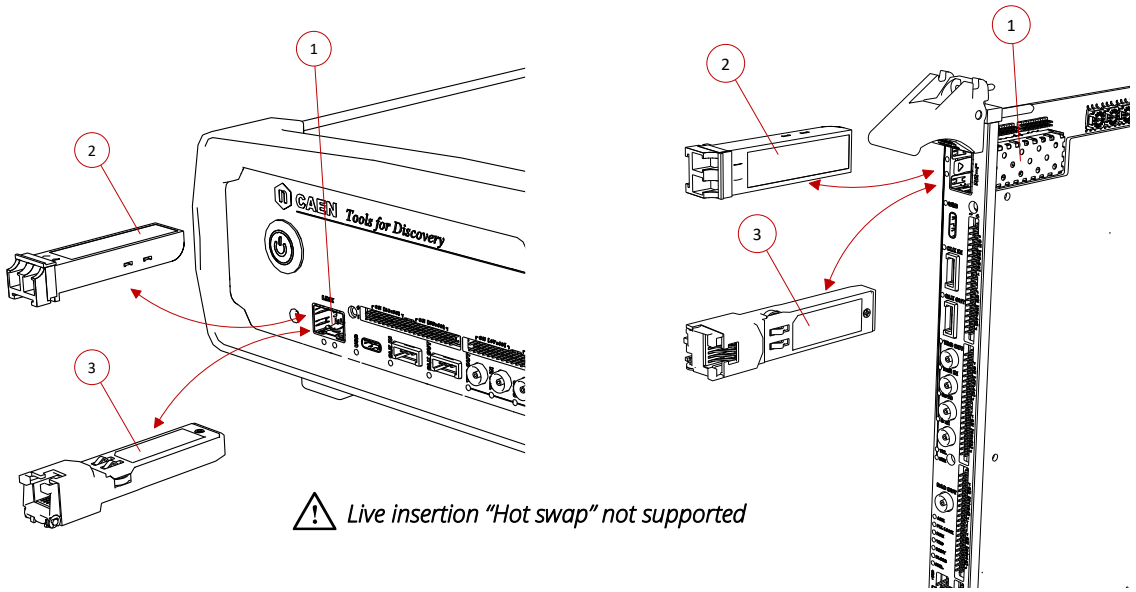
General Purpose I/O
TRG-IN / TRG-OUT / GPIO / S-IN
LEMO 00 connector

DAC-OUT LEMO 00 connector

LVDS I/O 16 differential pairs

LED mode
- OFF
- ON (COLOR)
- BLINKING (COLOR)

2740/2745 SFP+ receptacle for 1/10 GbE or Optical links



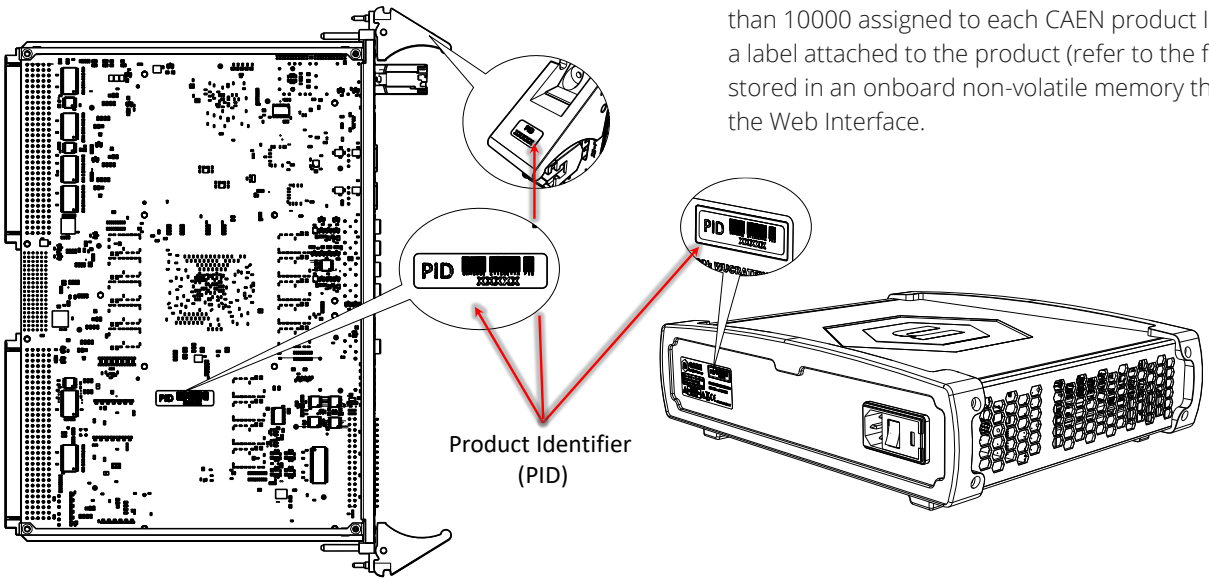
1 SFP+ receptacle for 1/10 GbE or Optical link

2 1/10 GbE Optical Transceiver
Type: AFBR-710DMZ Manufacturer: Avago

3 1 Gb Ethernet Transceiver
Cisco Compatible 1000Base-T Copper SFP (mini-GBIC) Transceiver

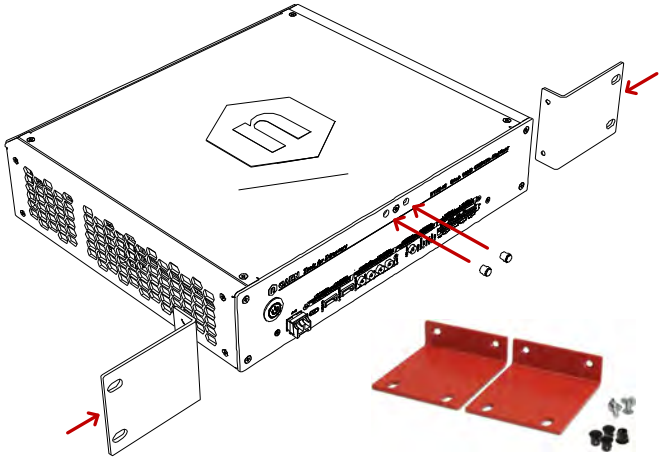
2740/2745 PID (Product Identifier)

PID (Product Identifier) is a unique incremental number greater than 10000 assigned to each CAEN product It can be found on a label attached to the product (refer to the figure) and is also stored in an onboard non-volatile memory that can be read via the Web Interface.



Rack Mounting:

Desktop digitizers (DT5740x/DT5745x) can be rack mounted using 2 brackets included in the product-kit.



A372F

64 channel 2.54mm Male Header Connector Adapter

The A372F adapter is compliant to all the form factors of the 2740 digitizer. It mechanically adapts to 2.54mm header from the 2mm header mounted on the digitizer, independently of the differential or single-ended standard of the 2740 analog channels.

Dedicated metal supports fixed by screws give stress resistance when plugged in the digitizer inputs.

A372M

64 channel MCX Coax Connector Adapter for SE signals

The A372M applies to the 64-channel 2740 Digitizer Family. It must be used with the single-ended input 2740 models and adapts to MCX Coaxial from the 2mm header mounted on the digitizer.

Metal supports fixed by screws give stress resistance when the adapter is mounted in the 2740 digitizer inputs.

A319A

Clock & Sync cable assembly

The A319A is a cable assembly for the Clock and Sync signal distribution in 2740 Digitizer Through the front panel CLK-OUT / CLK-IN daisy chain, this 4-contact cable carries two differential signals from one digitizer to another to synchronize multiple boards.

A319B

Clock cable assembly from 2740 series to Standard Digitizers

The A319B is a cable assembly for the Clock signal distribution between non homogenous digitizer series, matching the 3-contact connector on the Standard Digitizer to the 4 -pin connector on the 2740 Digitizer Series. Through the front panel CLK-OUT / CLK-IN daisy chain, this cable carries the differential clock signal from one digitizer to another to synchronize multiple boards .

A954

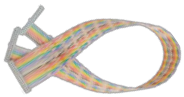
Cable assembly 2.54mm 34 pin female to two 2.54mm 16 pin female - 50 cm

A952

Cable assembly 2.54mm 34 pin female to 2.54mm 34 pin female - 50 cm

A316

Cable assembly 2.54mm 2-pin header female - 5 cm



A953

Cable assembly 2.54mm 34 pin female to two 2.54mm 34 pin female – 50 cm

µ-crate

Desktop single-slot VME64X Crate

- Mechanical compatibility: 1-unit VME 6U x 160 mm modules
- Standard power: 10.5 A @+3.3 V, 10 A @+5 V, 2 A @+12 V, 2 A @-12 V
- Fan speed control:
  - Manual adjustment via hardware button (high/low state)
  - Automatic control available only with Digitizer 2.0 series
- Mains power: 100 - 240 V AC (130 W) @ 50 / 60 Hz
- Includes a 19" rack mount kit adapter

The **µ-Crate** is a mains-powered desktop device integrating a low-noise cooling vents system. The desktop form factor can be optionally converted into a 19" rack thanks to the included metal brackets.

The single-slot backplane supports VME64 and VME64X CAEN boards of the Digitizer 1.0, Digitizer 2.0 Families, the V2495 Programmable Logic Unit, as well as other CAEN boards. Only VME Modules (one-unit, 6U x 160mm) with direct connection on the front panel (via USB-2.0/3.0, CONET optical link or 1/10 GbE) and/or not requiring VME bus control (VME protocols not supported) are compatible with the µ-Crate.

The images above show the µ-Crate product with a Digitizer from the 2.0 Family (VX2740) installed, as well as the two possible configurations: Desktop and rack-mountable (using the two brackets included in the sales kit).

Ordering Option

Description	Code
V2740 - 64 Ch 16 bit 125MS/s Digitizer, Diff	WV2740XAAAAA
V2740B - 64 Ch. 16 bit 125 MS/s Digitizer, SE	WV2740BXAAAA
VX2740 - 64 Ch 16 bit 125MS/s Digitizer, Diff	WVX2740XAAAA
VX2740B - 64 Ch. 16 bit 125 MS/s Digitizer, SE	WVX2740BXAAA
DT2740 - 64 Ch 16 bit 125MS/s Digitizer, Diff	WDT2740XAAAA
DT2740B - 64 Ch. 16 bit 125 MS/s Digitizer, SE	WDT2740BXAAA
V2745 - 64 Ch. 16 bit 125 MS/s Digitizer with Programmable Input Gain, Diff	WV2745XAAAAA
V2745B - 64 Ch. 16 bit 125 MS/s Digitizer with Programmable Input Gain, SE	WV2745BXAAAA
VX2745 - 64 Ch. 16 bit 125 MS/s Digitizer with Programmable Input Gain, Diff	WVX2745XAAAA
VX2745B - 64 Ch. 16 bit 125 MS/s Digitizer with Programmable Input Gain, SE	WVX2745BXAAA
DT2745 - 64 Ch. 16 bit 125 MS/s Digitizer with Programmable Input Gain, Diff	WDT2745XAAAA
DT2745B - 64 Ch. 16 bit 125 MS/s Digitize with Programmable Input Gain, SE	WDT2745BXAAA
Personalization	
x2740B Customization 10k Ohm Zin	WPERS2740B10
x2745B Customization 10k Ohm Zin	WPERS2745B10
Accessories	
A372F - 64 channel Adapter to 2.54mm Male Header Connector for Digitizer Series 2.0	WA372FXAAAAA
A372M - 64 channel Adapter to MCX Coax Connector for Digitizer Series 2.0	WA372MXAAAAA
A319A - Clock & Sync Cable for Digitizers Series 2.0 interconnection (L=20cm)	WA319AXAAAAA
A319B - Clock Cable for Digitizer Series 1.0 to 2.0 interconnection (L=20cm)	WA319BXAAAAA
A954 - Cable assembly 2.54mm 34 pin female to two 2.54mm 16 pin female – 50 cm	WA954XAAAAAA
A316 - Cable assembly 2.54mm 2-pin header female – 5 cm	WA316XAAAAAA
A952 - Cable assembly 2.54mm 34 pin female to 2.54mm 34 pin female – 50 cm	WA952XAAAAAA
A953 - Cable assembly 2.54mm 34 pin female to two 2.54mm 34 pin female – 50 cm 16pin each used only	WA953XAAAAAA
µ-Crate - Desktop single-slot VME64X Crate	WUCRATEX001A

2740/2745
Digitizer Family

open FPGA

16bit 125 MS/s

DESKTOP RACK VME Form Factor

1/10 GbE

USB 3.0

VGA

WEB INTERFACE

CAEN S.p.A.
Via Vetraia 11 55049 - Viareggio - Italy
Phone +39.0584.388.398
Fax +39.0584.388.959
info@caen.it - **www.caen.it**

CAENsn SAS
Gare du Nord Business Centre 14,
Rue De Dunkerque 75010 Paris - France
info@caen-sn.fr - **www.caen-sn.fr**

CAEN GmbH
Brunnenweg 9 64331 Weiterstadt - Germany
Phone +49 (0)212.254.4077
Mobile +49 (0)151.16.548.484
info@caen-de.com - **www.caen-de.com**

CAEN Technologies, Inc.
1 Edgewater Street - Suite 101
Staten Island, NY 10305 - USA
Phone +1.718.981.0401
Fax +1.718.556.9185
info@caentechnologies.com
www.caentechnologies.com

CAENspa India Private Limited
B205, BLDG42, B Wing, Azad Nagar Sangam CHS,
Mhada Layout, Azad Nagar, Andheri West
Mumbai, Maharashtra 400053 - India
info@caen-india.in - **www.caen-india.in**

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