N6741

32 Ch Peak Sensing ADC

NIM	32	1k, 2k, 4k, 8k, 16k
Package	No. of Inputs	Resolution (channels)

The N6741 is a 32-channel digital peak-sensing ADC in a 1-unit-wide NIM module. Its single-ended inputs use a 68-pin ERNI SMC connector (Zin: 2.5 kΩ) and accept positive or negative signals with software-selectable 4 Vpp or 8 Vpp full-scale range, or 3.75 Vpp and 7.5 Vpp with sliding scale enabled. Common-gate conversion, digital peak detection and FLASH ADC architecture provide about 50 ns dead time after gate closure. It offers 1k, 2k, 4k, 8k or 16k conversion gain, programmable zero suppression, a 1024-event buffer, and USB2.0 or optical-link readout.

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Overview

Product Highlights

- 1-unit wide NIM Module
- 32 input channels, single-ended, with 68-pin ERNI SMC connector (Zin: 2.5 kΩ)
  - Accepts positive and negative inputs
  - 4 Vpp or 8 Vpp Full Scale Range software selectable (3.75 Vpp and 7.5 Vpp when sliding scale is enabled)
- Low dead time (about 50 ns after the previous gate closes)
- Zero suppression with programmable threshold
- USB2.0 and Optical link (CAEN CONET proprietary protocol) communication interfaces
- Firmware upgradable by the user
- 1k, 2k, 4k 8k, 16k Peak Sensing ADC
- Common Gate mode (32 channels converted at once) with linear gate width or programmable by software
- Sliding scale algorithm for DNL reduction
- Multi-Event Buffer (1024 events)
- Windows and Linux drivers, C and LabVIEW libraries, demo software

Product Description

AT A GLANCE	
Package	**NIM**
No. of Inputs	**32**
Resolution (channels)	**1k, 2k, 4k, 8k, 16k**
Conversion Time (µs)	**0.1**
Full Scale Range (V)	**4**
Multi Event Buffer size	**1024 events / ch**

The **N6741** is a **Digital Peak Sensing ADC** belonging to a new generation of detector readout systems based on a mixed analog-digital acquisition chain, combining a high channel density (**32 channels**) and a **low dead time**. The FLASH ADC architecture makes it possible to achieve an extremely low conversion time of the pulse peak, so new conversions take place less than 50 ns after the previous gates close.

Conversion gain ranges **from 1k up to 16k** channels with a low differential non-linearity (DNL) thanks to the *sliding scale method*.

Receiving the typical slow signal from a **Charge Sensitive Preamplifier** followed by a **Shaping Amplifier** (e.g. CAEN N1068), the FPGA identifies the peak of the pulse within a gate by means of digital filters. *The acquisition is common to all channels and takes place as soon as the GATE arrives.* The energy value together with the time of arrival of the event is first stored in a 1024 multi-event buffer and made available for the readout by USB or optical link interface (Daisy-chainable). Both the energy spectrum and the list of events is available through the software interface. Data throughput can be reduced by the Zero Suppression algorithm with a programmable threshold.

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Overview (continued)

The front panel hosts LEMO (NIM/TTL) inputs that can be used for the **GATE**, the event discard in case of pile-up (**REJ**), and the GATE propagation (**GPO**). The Gate can be linear (same width as the external signal) or re-formed with programmable width.

The N6741 is provided with drivers for the supported communication interfaces, C libraries, demo software for an easy board understanding. Firmware upgrade can be performed via optical link or USB by the user.

Technical Specifications

GENERAL	• Form Factor: 1-unit wide, NIM module • Weight: 870 g
ANALOG INPUT	Channels: 32 channels, Single-ended Offset: The Sliding Scale automatically manages the DAC for DC offset adjustment on each channel. Connector: 68-pin ERNI SMC with 1.27 mm pitch or 2 x 34 pin header-type male connector with 2.54 mm pitch Impedance: Zin = 2.5 kΩ Full Scale Range (FSR): • 4 Vpp (3.75 Vpp with sliding scale enabled) or 8 Vpp (7.5 Vpp with sliding scale enabled) • SW selectable
DIGITAL CONVERSION	• Resolution: 12 bits • Sampling Rate: 62.5 MS/s simultaneously on each channel
CONVERSION GAIN	1k, 2k, 4k, 8k, 16k
DEAD TIME	50 ns
MINIMUM RISE TIME	2 ns
INTEGRAL NON LINEARITY (INL)	< 0.05 % in the range of (1:99) % of the FSR
DIFFERENTIAL NON LINEARITY (DNL)	< 1 %
ZERO SUPPRESSION	Zero Suppression threshold common to 8-channel groups and programmable in steps of ADC counts over the entire FSR
GATE	Gate mode with linear gate width or programmable by software. The GATE signal is fed into the GATE LEMO connector. **Gate propagation:** Gate_IN/Gate_OUT propagation through the GATE/GPO LEMO connectors
MEMORY	Multi-event Buffer of 1024 events
DIGITAL I/O	

GATE (LEMO)
Front panel digital input of NIM/TTL logic: when high the event is acquired;
Z_{in} = 50 Ω

CLK-IN (AMP Modu II)
AC coupled differential input clock
LVDS, ECL, PECL, LVPECL, CML (single-ended NIM/TTL available by A318 adapter)
Jitter <100ppm requested

GPO (LEMO)
Digital output that automatically propagates the GATE input
NIM/TTL; R_t = 50 Ω

REJ (LEMO)
Front panel digital input of NIM/TTL logic: when high the event is rejected
Z_{in} = 50 Ω

TIME STAMP	48-bit counter, 8 ns step, 16 ns resolution, 625 h range
ADC & MEM. CONTROLLER	Altera Cyclone EP1C16 (one FPGA serves 16 channels)

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Technical Specifications (continued)

COMMUNICATION INTERFACE	
USB • USB 2.0 compliant • Transfer rate up to 30 MB/s	**Optical Link** • CAEN CONET proprietary protocol • Up to 80 MB/s transfer rate • Daisy chainable: it is possible to connect up to 8 or 32 ADC modules to a single Optical Link Controller (respectively A2818 or A3818)

DPP FW SUPPORTED	Peak Sensing firmware
FIRMWARE UPGRADE	Firmware can be upgraded via USB/Optical Link
SOFTWARE	General purpose C libraries, configuration tools, readout software (Windows and Linux support)
POWER CONSUMPTIONS	3.6 A @ +6 V (typ.); 500 mA @ -6 V (typ.)

Ordering Information

ORDERING CODE	DESCRIPTION
WN6741XAAAAA	N6741 32ch Peak Sensing ADC

1. Ordering codes and descriptions are reproduced from the product record. Availability is confirmed at order entry.

Accessories

A317 — Cable assembly for Clock distribution 3-pin AMPMODU IV female terminations – 18 cm / 25cm

A318 — Adapter for Clock signal FISCHER S101A004 male to 3-pin AMPMODU IV female – 10 cm

A385 — Adapter 2.54mm 34-pin female to 16x LEMO 00 female (or MCX male) – 50 cm / 1 m

A746D — Patch panel 32x LEMO 00 female to 1.27mm 68-pin ERNI SMC female

A952 — Cable assembly 2.54mm 34 pin female to 2.54mm 34 pin female - 50 cm

A4818 — USB 3.0 to CONET2 Adapter

A5818 — CONET2 Controller based on PCI Express Gen 3 interface

AI2700 — Optical Fiber Series

Related Products

N957 — 8k Multi-Channel Analyzer

N1068 — 16 ch Programmable Spectroscopy Amplifier and 16ch CFD

NIM8302P — 5U 5 slot 150 W Portable Crate

NIM8303 — 5U 12 slot 300/600 W Crate

NIM8304 — 7U 12 slot smart fan unit Switching 2000 W Crate

NIM8305 — 2 Slot Switching 450 W Mini Crate

NIM8306 — 2 Slot Switching 750 W Mini Crate

V1741 — 64 Ch Peak Sensing ADC

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