R5560

128 Channel 14 bit 125 MS/s Open FPGA Digitizer

14	125	128+6
Resolution (bits)	Max Sampling Rate (MS/s)	No. of Channels

The R5560 is a 2U, 19" rack-mount open FPGA digitizer with 128 channels, 14-bit resolution and 125 MS/s sampling. Based on a Xilinx Zynq-7000 SoC, it provides programmable real-time processing for large detector arrays, including PMTs, segmented HPGe and position-sensitive 3He tubes with the R1443 preamplifier. It supports 2 Vpp input dynamics, configurable LVDS, NIM and TTL digital I/Os, board-to-board synchronization through a single CAT5e cable, and USB3.0, Ethernet and optional Optical Link connectivity. A 2.4” touch screen provides configuration and status control.

Overview

Product Highlights

- 128 channels, 14-bit @125 MS/s Digitizer
- 2U, 19” Rackmount unit with automatic fan control
- Specifically designed for the readout of position-sensitive 3He tubes in combination with R1443 preamplifier
- Fully supported by SCI-Compiler for easy FPGA programming (Firmware runtime license included onboard)
- Board-to-board synchronization with a single CAT5e cable.
- Maximum flexibility: USB3.0, Ethernet, and Optical Link (OPTIONAL) connectivity, to support remote management as well as extreme fast data flow
- Based on powerful Xilinx Zynq-7000 SoC with open FPGA
- Full-featured readout system for the readout of large arrays of detector (PMTs, segmented HPGe, Gas Tubes, …)
- 2 V_{pp} input dynamic
- Easily scalable
- Configurable digital I/Os to interface with external systems
- 2.4” touch screen display for quick configuration and status control

Product Description

AT A GLANCE	
Resolution (bits)	**14**
Max Sampling Rate (MS/s)	**125**
No. of Channels	**128+6**
Package	**rack mount 19 -2U**
Bandwidth (MHz)	**60**
Full Scale Range (V)	**2**

The **R5560** is a 2U, 19" rack-mount 128 Channels 14-bit 125MS/s Open FPGA Digitizer Family, designed to attain programmable data processing capabilities.

The R5560 is designed for the readout of large **arrays of detectors** (PMTs, segmented HPGe, ^{3}He tubes, …) using a **customizable platform.** In fact, it is possible to take advantage of the powerful SoC mounted onboard to write a **custom pulse processing algorithm** on the open FPGA as well as build a middleware/software that fits the needs of the application of interest.

The board can manage simultaneously a large number of **digital** (LVDS, NIM, TTL) and **analog** signals, allowing to implement many functionalities required by physics experiments: signal digitization, complex trigger logic, Pulse Height Analysis with MCA capabilities, Time Tagging, Pulse Shape Discrimination, etc.

It is an optimal solution for **large experiments,** usually requiring fast digitization of analog signals and usage of several digital lines to interface with external systems. The board supports **multi-board synchronization** through a single CAT5e cable, with the possibility scale up to thousands of channels**.** Moreover, the **rack-mount** form factor simplifies the experimental setup in case of multi-board systems, where an effective space management is often a constraint. The usage of differential inputs on RJ45 connectors **optimizes the cost for the installation,** reducing the cabling cost.

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Overview (continued)

SCI-Compiler software, the CAEN block-diagram-based firmware generator and compiler, helps in programming the FPGA to develop intensive real-time data processing. A free and open-source demo **readout software** is available to manage the standard pulse height analysis firmware implementing energy measurements using a trapezoidal filter.

Applications includes:

Readout of the following detectors	• Neutron Detector (3He tubes, position sensing tubes) • HPGe, Segmented germanium detector • Array/matrix of PMTs • Position sensing detectors (for application like gamma camera) with real-time position reconstruction • CdTE and CZT detector • Neutron scintillator detectors with Gamma Neutron discrimination
Readout of mixed signals ASICs	
Nuclear Spectroscopy	
High Energy Physics	
Imaging with multichannel detectors	

Developed in collaboration with Nuclear Instruments.

Technical Specifications

General	Form Factor : 19”, 2U Rack-mount Dimensions (HxWxL): 88 x 482.0 x 367.0 (396 with handles) mm

Power Requirements

- Voltage: 100-240 V_{ac} ± 10%
- Frequency: 50/60 Hz
- Typ. Power consumption: 0.5 A @ 220 V_{ac}

Analog Input

- Channels: 128 channels Differential
- Impedance: Z_{diff} = 100 Ω
- Connector : 32 x CAT5e RJ45
- Full Scale Range: 2 Vpp
- Bandwidth: 125MHz

Digital I/Os

- Channels: 128 Differential
- Impedance: Z_{diff} = 100 Ω
- Connector: 4 x VHDCI
- Coupling: DC
- Signal Type: LVCMOS 2.5V, LVDS, BLVDS

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Technical Specifications (continued)

Digital Conversion	• Resolution: 14 bits • Sampling Rate: 125 MS/s Simultaneously on each channel
Clock Generation	**Clock source: internal/external** On-board programmable PLL provides generation of the main board clocks from an internal (25 MHz local Oscillator) or external (rear panel CLK-IN connector) reference External Clock from Sync connector with clock and sync propagation Clock recovery and propagation from optical link with integrated jitter cleaner

LEMO Digital I/O

USER IO 0…5 (LEMO)
- Programmable Digital I/O:s can be used as Trigger, Start, Busy
- IN/OUT
- Single-ended, Z_{in} / Rt = 50 Ω

Trigger	Trigger Source: *Internal/External*: managed by the default firmware; *Complex trigger logic*: implementable by the user on the open FPGA. Trigger Propagation: Through LEMO and Sync Connector. Trigger Time Stamp: *Default FW*: 32-bit counter, 8 ns resolution, 26-day range; *Custom FW*: defined by the firmware design.
Open FPGA	4x Xilinx Zynq-7000 SoC: Z-7030 (R5560A, R5560SEA) Z-7035 model (R5560B, R5560SEB)
Memory	• 1 GByte of memory for list readout on each SoC • Up to 8kS/ch for simultaneous waveform readout

Communication Interface

All readout interfaces allow to perform the same task at different speed and using different media. They can be used independently or simultaneously.
The different readout interface allows to integrate the R5560 in existing experimental environment.
- Ethernet (readout): 4 x 1 Gbps (4 Gbps cumulative speed)
- Ethernet (slow control): 1 Gbps (slow control is an additional port, not required if the fast readout ethernet is used)
- Parallel TTL/LVDS Readout: Readout through the VHDCI digital I/O on custom protocol
- USB 3.0: 1 x USB 3.0 readout
- Optical Link: Slots for 8 x 10Gbps SFP+ transceivers (communication protocol not implemented by default): can operate as point-to-point or in daisy chain mode

Firmware	Default: Waveform recording and Pulse Height Analysis, Ethernet communication Custom: Use SCI-Compiler to develop your own firmware.
Firmware Upgrade	Firmware can be upgraded via Ethernet, USB 3.0 or USB 2.0 debugger (on-the-fly)
Software	• Open Hardware Readout Software to manage the default firmware • SCI-Compiler for custom firmware development

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Ordering Information

ORDERING CODE	DESCRIPTION
WR5560AXAAAA	R5560A 128 Ch. 14 bit 125 MS/s Digitizer-7030
WR5560BXAAAA	R5560B 128 Ch. 14 bit 125 MS/s Digitizer-7035

1. Ordering codes and descriptions are reproduced from the product record. Availability is confirmed at order entry.

Related Products

R1443 — Preamplifier Unit for He3 Tubes

R5560SE — 128 Channel 14 bit 125 MS/s Open FPGA Digitizer

Software & Control Tools

Sci-Compiler — Graphical Programming Language for CAEN Open FPGA Boards